# AN EMPIRICAL METHODOLOGY FOR FOUNDRY SPECIFIC SUBMICRON CMOS ANALOG CIRCUIT DESIGN

by

Wilfredo Rivas-Torres

A Dissertation Submitted to the Faculty of the

College of Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

Florida Atlantic University

Boca Raton, Florida

December 2013

AN EMPIRICAL METHODOLOGY FOR FOUNDRY SPECIFIC SUBMICRON CMOS ANALOG CIRCUIT DESIGN

by

Wilfredo Rivas-Torres

This dissertation was prepared under the direction of the candidate's dissertation advisor, Dr. Zvi Roth, Department of Electrical Engineering and Computer Science, and has been approved by the members of his supervisory committee. It was submitted to the faculty of The College of Engineering and Computer Science and was accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

SUPERVISORY COMMITTEE:

_____
Zvi Roth, Ph.D.
Dissertation Advisor

_____
Ali Zilouchian, Ph.D.

_____
Nurgun Erdol, Ph.D.
Chair, Department of Electrical Engineering and Computer Science

_____
Perambur Neelakanta, Ph.D.

_____
Ravi Shankar, Ph.D.

_____
Mohammad Ilyas, Ph.D.
Dean, College of Engineering and Computer Science

_____
Ankur Agarwal, Ph.D.

_____
Lorenzo Ponce De Leon, Ph.D.

_____
Barry T. Rosson, Ph.D.
Dean of the Graduate College and Vice President for Research

_____
Date

# ACKNOWLEDGEMENTS

The author would like to thank TowerJazz for providing the CA18HB process design kit (PDK) that was used in this research for all ADS analyses and simulations. I want to specially thank Samir Chawdhury for always being available to answer my questions about the TowerJazz process and for facilitating the signing of the agreement between FAU and TowerJazz. A very special thank you to my family (Haydee, Wilfredo S. and Winny) that endured this research process and without their love, support and especially their patience I would have never been able to complete it.

# ABSTRACT


| | |
|---|---|
| Author: | Wilfredo Rivas-Torres |
| Title: | An Empirical Methodology for Foundry Specific Submicron CMOS Analog Circuit Design |
| Institution: | Florida Atlantic University |
| Dissertation Advisor: | Dr. Zvi Roth |
| Degree: | Doctor of Philosophy |
| Year: | 2013 |



Analog CMOS amplifiers are the building blocks for many analog circuit applications such as Operational Amplifiers, Comparators, Analog to Digital converters and others. This dissertation presents empirical design methodologies that are both intuitive and easy to follow on how to design these basic building blocks. The design method involves two main phases. In the first phase NMOS and PMOS transistor design kits, provided by a semiconductor foundry, are fully characterized using a set of simulation experiments. In the second phase the user is capable of modifying all the relevant circuit design parameters while directly observing the tradeoffs in the circuit performance specifications. The final design is a circuit that very closely meets a set of desired design specifications for the design parameters selected. That second phase of the proposed design methodology utilizes a graphical user interface in which the designer moves a series of sliders allowing assessment of various design tradeoffs. The theoretical

basis for this design methodology involves the transconductance efficiency and inversion coefficient parameters. In this dissertation there are no restrictive assumptions about the MOS transistor models. The design methodology can be used with any submicron model supported by the foundry process and in this sense the methods included within are general and non-dependent on any specific MOSFET model (e.g. EKV or BSIM3). As part of the design tradeoffs assessment process variations are included during the design process rather than as part of some post-nominal-design analysis.

One of the central design parameters of each transistor in the circuit is the MOSFET inversion coefficient. The calculation of the inversion coefficient necessitates the determination of an important process parameter known as the Technology Current. In this dissertation a new method to determine the technology current is developed. Y-parameters are used to characterize the CMOS process and this also helps in improving the technology current determination method. A study of the properties of the technology current proves that indeed a single long channel saturated MOS transistor can be used to determine a fixed technology current value that is used in subsequent submicron CMOS design. Process corners and the variability of the technology current are also studied and the universality of the transconductance efficiency versus inversion coefficient response is shown to be true even in the presence of process variability.

DEDICATION

To:

Haydee for all her uncompromising love through good and bad times, to my grandma (Jesusa) who taught me how to laugh and what real courage is all about, I miss you and to Peluzo, if our love could have saved you then you would have lived forever… 

AN EMPIRICAL METHODOLOGY FOR FOUNDRY SPECIFIC SUBMICRON CMOS ANALOG CIRCUIT DESIGN

LIST OF TABLES

LIST OF FIGURES

# SUMMARY OF RESEARCH CONTRIBUTIONS

Classical CMOS design is based on square law equations that form the basis for CMOS Level 1 modeling. Such approach is thought to be adequate down to channel length of 4 μm [9 chap. 16, 11 ss. 3.4]. Modern day technology reaches down to channel length of 0.022 μm. Present day MOSFET models are very complex and do not lend themselves to easy design equations that can be used for analytic analog CMOS design [7]. Analog designers are thus left with no easy closed form equations to use for their designs as they did in the micron era, which proves to be a huge challenge. The only exceptions are users of foundry models that support the EKV model of a MOSFET. These users can benefit from the relative compactness of the EKV model. Most users however do not have access to the EKV model parameters. The main goal of this thesis is to provide the circuit designer with a structured design methodology that is more empirical and graphical, based on Transconductance Efficiency ($g_m/I_D$) and Inversion coefficient (IC) that is both intuitive and easy to follow. Several basic and more advanced CMOS amplifiers are used to demonstrate the usefulness of these new methodologies.

In order to meet the above main goal a search technique to determine technology current ($I_0$) versus channel length and drain to source voltage is developed. This technique is independent of any specific CMOS submicron model and therefore is generic in the sense that it is not MOS model dependent. A good estimate of the technology current is a prerequisite for determining the inversion coefficient. The

inversion coefficient and the chosen channel length are thereafter used along with Binkley's MOS Operating Plane to guide the circuit design process.

Technology current drain to source voltage, channel length and process corner dependencies are studied in this thesis. The results indicate that indeed $I_0$ depends not only on the channel length but also on the drain to source voltage for a proper determination of $I_0$. The results of $I_0$ versus process corners are then used to prove that indeed the transconductance efficiency $g_m/I_D$ is universal in nature even across process corners.

MOS characterization techniques using Y-parameters that simplify $g_m/I_D$ and $g_{ds}/I_D$ measurements are developed. The determination of the linearized Y-parameters of a MOS device allow for the simultaneous measurement of $g_m$ and $g_{ds}$ which in turn reduces the number of simulations and measurements needed to fully characterize MOS transistors. Using Y-parameters also simplifies the $I_0$ determination process and eliminates the need to numerically calculate $g_m$ using differentiation (i.e. $g_m=dI_D/dV_{GS}$). This characterization process is central to the design methodology developed.

In this dissertation step by step design techniques based on Transconductance Efficiency and Inversion Coefficient (IC) for basic CMOS amplifiers (Common Source and Cascode) and more advanced amplifiers (Differential Amplifiers and OTAs) were developed. Designers who follow the design methodology can now predict the performance of these circuits from a set of design parameters. The designs are built into the simulator and the resulting performance is shown to match closely the predicted performance based on graphs extracted from MOSFET foundry data.

As a proof of concept it is shown for CS NMOS amplifiers with PMOS current source load that MOS tolerances can be incorporated during the design phase itself. As far as the author knows this is the first work in which such an approach is demonstrated. It is done by including in the design techniques process variability as part of the analog CMOS design methodology. This process variability is accounted for by running the same characterizations as in done for a nominal process at the corner (fast and slow). The designer is then presented with the information of what happens at the process corners with the design variable values selected. This provides the designer the ability to assess process variability in an early stage of the design process.

# 1.0 INTRODUCTION

## 1.1 Motivation, Scope and Objectives of the Research

In many US universities CMOS design engineering courses and in many electronics textbooks MOSFET Level 1 model equations are still in popular demand. Everyone knows that Level 1 became obsolete more than 30 years ago. Level 1 Design techniques are inadequate for analog CMOS design in present day submicron technology not even as ways to predict approximately the design outcomes. In current circuit design research literature and in modern day industry practices other analog electronics design techniques have been used but such techniques have not yet percolated down to mainstream undergraduate and graduate electronics education.

One can find in the literature methods that are based on macro-modeling and geometric programming [21]. These techniques involve the formulation of monomial and polynomial expressions that are the bases for the objective and constraints functions needed in the formulation of the geometric programming circuit design problem.

A common industry approach to CMOS design is to use simulation packages with tuning and optimization capabilities. Simulator optimizers are typically given with design goals (in the form of equality and inequality conditions) that match a set of desired circuit performance specifications. Such optimizers are also given with a set of design constraints. These optimizers search for feasible solutions. Search methods range from direct search, through gradient methods to methods that can avoid local minima. The

designer may take advantage of these advanced capabilities but this can lead to many hours spent in front of the simulator "tweaking" earlier designs with the hope of creating new designs. Based on the author's industry experience these techniques tend to leave the designers without sufficient intuitive sense as to how to improve the design if later needed due to unexpected circumstances such as a change in circuit performance requirements towards the latter part of the design cycle. This may lead to "back to more analysis and simulations" which is particularly frustrating.

There is a need for a methodology that does not depend on any specific MOSFET model being used by the foundry. That is we seek a generic methodology that is MOSFET model independent since most modern CAD models are too complex for manual calculations. This work investigates the systematic design of Analog CMOS circuits using the transconductance efficiency and inversion coefficients parameters as proposed by Binkley, et al. [3,7]. However, unlike Binkley's design methods that rely heavily on analytical expressions provided by the EKV model and on foundry supported EKV model parameters our method will be model independent. The main motivation for the present work is to develop a systematic empirical design methodology that is MOSFET model independent.

The scope of this research is:

- To develop a systematic design methodology that covers basic amplifier circuits that are the building blocks for more complex systems.
- Develop model free techniques in the sense that any foundry process, that can provide a model design kit compatible with the simulator being used, will work and allow for the design of these analog CMOS circuits.

- These design techniques only require that the designer select basic design parameters like the transistor current, transistor node voltages, channel length and transistor inversion level from a set of sliders in the user design interface.

The following are the objectives that we have set for this work:

- Facilitate the determination of the inversion level of MOSFET transistors by developing techniques for the determination of the so called Technology Current.
- Characterize foundry process models to develop a systematic design methodology for analog CMOS circuits.
- Ability to see the values of the design performance specifications along every step while tuning design parameters. These techniques include active consideration of the process variability that allows the designer to quantify how much the performance of the design may vary from a nominal.
- Provide the designer with an easy way to assess analog CMOS circuit design tradeoffs.
- Five different amplifiers are designed and their tradeoffs are analyzed. The tradeoffs include such important parameter as channel length and inversion coefficient. The main design performance tradeoffs in this work are voltage gain, output resistance and bandwidth.
- We show that the MOS Operating plane is an appropriate tool to guide the complete design of CMOS analog circuits. Additional parameters not included in the MOS Operating plane such as drain to source voltage ($V_{DS}$) and bulk effect due to non-zero bulk source to bulk voltage ($V_{SB}$) are added.

## 1.2 Transconductance Efficiency

Design techniques that center around the Transconductance Efficiency ($g_m/I_D$) of each transistor, championed by Binkley and many other present day analog design researchers appear to resolve many of the above difficulties. This technique was first introduced in a paper by Silveira, Flandre and Jaspers [5] in which they designed an OTA based on the transconductance efficiency concept. In this family of design techniques the channel width (W) is replaced as a design variable by the MOS Inversion Coefficient (IC). This technique is further improved by the presentation of the MOS Operating Plane that provides both intuitiveness and guidance necessary for the design of Analog CMOS circuits [3]. Many of the proponents of these techniques have done so in the context of the EKV model. To be specific, the EKV MOSFET model has been used both to provide theoretical justifications to Binkley's Operating Plane, and to provide relatively simpler model equations used to implement formulas in spreadsheet tables that are part of a simulation-based analog design. While the EKV model is still a fairly modern CMOS compact model it is not in popular use by foundries. There exist literature sources that relate the EKV model with some of the more established advanced models (e.g. BSIM3) [18, 19] which allows designers and researchers to utilize the EKV model if they know explicitly all the other model parameters and how to convert those to EKV model parameters.

Advanced complex MOS models (e.g. BSIM4, PSP, etc.) which may have hundreds of parameters, many of those are abstract curve-fitting type parameters, do not help the design process intuitiveness either. While computationally efficient and accurate in predicting MOS behavior in simulation mode they are too complex to easily be used

for any analytical computer-aided design effort. This is why the EKV model still has great appeal among researchers because it facilitates hand calculations that provide design intuition for many CMOS designs [4, 8].

In [3] the authors present a spreadsheet method that allows the designer to provide the values of inversion coefficient, channel length, and drain current. The program (implemented in Microsoft Excel) calculates such parameters as transconductance $g_m$, intrinsic gain, noise density, 1 dB gain compression and more. The design spreadsheet utilizes model parameters that are fixed across device geometry and bias conditions for NMOS and PMOS devices. This is the first approach that seems to attempt to give the designer a practical and intuitive design tool based on transconductance efficiency and inversion coefficient. There are two main problematic issues with this approach:

i) This method still depends on the EKV model or some future development that may include some advanced models such as BSIM. In other words this method is still dependent on the specific CAD model being used and is not generic. That is, if the model changes the Excel worksheets used as part of this method must be redone.

ii) Using the spreadsheet results for a single transistor, the designer has to then take this information and determine if the parameters obtained fit the overall circuit design goals. That is, whether the transconductance value obtained from the spreadsheet is or not acceptable for the design. This process results in a tedious trial and error cycle as it needs to be executed for each transistor. The process can become extremely cumbersome for analog CMOS circuit designs that may require a large number of transistors, as most surely do.

Our research provides on the other hand techniques that do not have these limitations. An important part of our work involves making no assumptions in terms of the MOS behavior. Therefore we stay away from any MOS simplification or macro-modeling. This is possible by using the same foundry design kits that are provided to industry designers. A partnership between FAU and TowerJazz Semiconductor, Inc. had been formally established so that the TowerJazz foundry design kit could be used as part of this work. A TowerJazz 0.18 um design kit has been made available to Florida Atlantic University (FAU) and was used exclusively in this research. This means that all designs must obey the TowerJazz process requirements [14, 15]. The emphasis of this work is on amplifiers that are the basic building blocks for more complex systems in the audio and video frequency range.

## 1.3 Relevant Literature

The $g_m/I_D$ CMOS design methodology is an attractive design methodology because it allows the design to take place over the entire MOS operating region (i.e. from weak through strong inversion) [1, 2]. This family of design methods can be divided into two types; (i) analytical and (ii) experimental. The analytical approach is based on device models that manage to capture correctly all the physical phenomena at the desired technology while being simple enough analytically to allow for manageable design formulas (e.g. EKV model). References [3, 4, 7, and 8] advocate this approach based on the EKV model. The experimental approach on the other hand uses device characteristic data generated by a simulator (e.g. SPICE) or obtained from measured results. Reference [22] uses this approach based on simulation results using HSPICE and BSIM3 models.

The analytical $g_m/I_D$ design methodology in contrast utilizes equations motivated by the EKV MOS model.

In 1993 Vittoz published "Micropower Techniques" [1] in which he defined the inversion coefficient (IC). The inversion coefficient provided a precise way to characterize a MOS device inversion region of operation (i.e. Weak, Moderate or Strong) [1, 12]. A study that showcased for the first time the transconductance efficiency as the basis for Analog CMOS design is by Silveira, et al. in 1996 [5]. In that paper the authors used the transconductance efficiency versus "normalized current" ( $I_n=I_D/(W/L)$ ) to design a SOI CMOS OTA. In 2002 Foty, Bucher and Binkley [2] demonstrated that the transconductance efficiency versus inversion coefficient is a fundamental characteristic of a MOS transistor. They also showed how the technology current ($I_0$) can conceptually be determined from this curve ($g_m/I_D$ vs. IC). Binkley, et al. in their 2003 paper [3] in presented the MOS operating plane, a tool that allows the assessment of the tradeoffs possible for a given MOSFET Transistor biased in saturation depending on the channel length and inversion coefficient. Further details are presented and explained in section 2.5.

Based on the EKV MOS model Binkley and others were able to determine an analytical expression for the MOS technology current and develop other important design equations useful for analog CMOS design. The methodology was implemented in a prototype CAD system (based on Microsoft Excel) permitting the designer to explore the MOS design space of drain current, inversion level, and channel length while observing a graphical view of MOS performances against selected goals. This allows the designer to optimize the sizing of individual MOSFETs (or related groups of MOSFETs). The device

optimizations, done before circuit simulations are conducted can minimize time consuming trial and error simulations. The final design sizes can finally be fine-tuned or confirmed using simulations with complete foundry models. The MOS spreadsheet is further presented and showcased in Binkley's book [7]. Other examples of the usefulness of the transconductance efficiency analytical design methodology are shown in [8, 16, 17, 20].

The $g_m/I_D$ experimental design method presented in [22, 24] is based on a graphical lookup approach. This methodology optimizes individual transistors based on three claimed to be fundamental plots that include the transit frequency, intrinsic gain and current density ($I_D/W$) as a function of $g_m/I_D$ and for several channels lengths. The experimental data is obtained from HSPICE operating point for a test MOS device in which the channel length is swept. In [24] the authors use the lookup table to design a low power OTA.

In reference [23] an analytical method based on the inversion factor (that is, the inversion coeficient) and $g_m/I_D$ is presented. A set of optimally designed basic building blocks are added to a library. The building blocks are designed based on the analytical method using the EKV model as the basis for the design of the basic blocks. A BSIM3 to EKV model converter is presented. This conversion is needed to utilize the EKV expressions for such parameters as $I_0$, inversion factor and transconductance effciency. A program called PADS then uses the library of basic blocks to complete the design.

Note: In this thesis neither the Spreadsheet used in [3] nor the PADS program were available for testing as part of this research.

Analog design optimization methods applicable to CMOS design can be divided into three groups; (i) Classical Optimization Methods, (ii) Global Optimization Methods and (iii) Convex Optimization and Geometric Programming Methods. Unfortunately in the literature many papers do not clearly specify which MOSFET models they used and it seems like these studies loosely used Level 1 modeling but this is not always clear. Classical optimization methods, such as steepest descent, sequential quadratic programming, and Lagrange multiplier methods, have been widely used in analog-circuit CAD. These methods can be traced back to the paper by Brayton et al [25] in which a 1981 survey of different optimization methods is presented. The classical methods can be used with complicated circuit models, including even full SPICE like simulations [13, 29]. The optimization cost function (aka error function) is the method used to evaluate how far away from the target at each simulation iteration the design is [9]. In its most general definition, the error function (EF) calculates the difference between the simulation and the specifications defined by the optimization goals. One possible formulation of the error function is shown below in general terms:

$$EF = \sum_{allGoals} Weight_i \left| simulation_i - goal_i \right|^P$$

Here the error function (EF) first determines the difference between the simulation ($simulation_i$) and the goals ($goal_i$) for all of the goals that have been defined. This difference is usually called a residual. Each residual is then raised to a power P, and the result is then multiplied by a weighting factor, $Weight_i$. The error function value is determined as the sum of all these terms.

Global Optimization methods are guaranteed to find the globally optimal analog-circuit design. Representative global optimization methods used in analog design are branch and bound [31] and simulated annealing [30, 32]. Branch and bound methods determine the globally optimal design because at each iteration they maintain a suboptimal feasible design and also a lower bound on the achievable performance. This enables the algorithm to terminate with complete confidence that the global design has been found within a given tolerance. Simulated annealing is extremely effective for problems involving continuous variables and discrete variables, as in simultaneous amplifier sizing problems. Simulated annealing is a probabilistic method for finding the global minimum of a cost function that may possess several local minima.

An optimization method for determining component values and transistor dimensions for CMOS operational amplifiers is performed in [26, 27, 28]. The method is based on a variety of design objectives and constraints that have a special form, i.e., they are posynomial functions of the design variables. As a result the analog CMOS design problem can be expressed as a special form of optimization problem called geometric programming, for which very efficient global optimization methods have been developed. As a consequence this method can efficiently determine globally optimal analog CMOS designs, or globally optimal trade-offs among competing performance measures such as power, open-loop gain, and bandwidth. This method yields completely automated synthesis of globally optimal CMOS designs. In [26] an operational amplifier architecture is designed (see Figure 1-8), showing in detail how to formulate the design problem as a geometric program. Optimal trade-off curves relating performance measures such as power dissipation, unity-gain bandwidth, and open-loop gain are constructed. The

method can be used to synthesize robust designs, i.e., designs guaranteed to meet the specifications for a variety of process conditions and parameters. In the two stage op-amp of Figure 1-1 there are 19 design variables [27]: W1 – W8, L1 – L8, Rc, Cc, and Ibias.

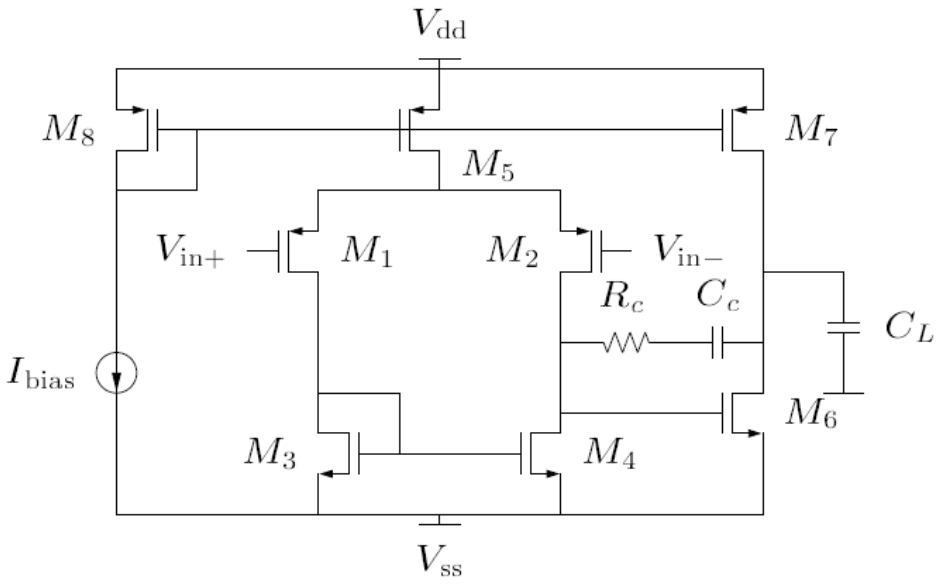



Figure 1-1 Two Stage Op-Amp in 0.5 µm Technology

The constraints for this problem are based on the design and process restrictions. Dimension constraints are:

Lmin ≤ Li ≤ Lmax
Wmin ≤ Li ≤ Wmax

These need to be expressed as posynomial, e.g. Li/Lmin ≤ 1. Symmetry constraints are:
W1 = W2
L1 = L2
W3 = W4
L3 = L4
Bias Transistor Matching Constraints are:
L5 = L7 = L8

Other bias constraints include that each transistor must remain in saturation over the specified common mode input ($V_{cm,min}$ and $V_{cm,max}$) and output voltage ($V_{out,min}$ and

$V_{out,max}$). The authors show that using the HPSICE simulator and BSIM3.1 models that they get an OpAmp gain of 83 dB where there model had predicted 80 dB. This is considered a good agreement between their macro model and the more accurate BSIM3.1

## 1.4 Thesis Organization

The remainder of the dissertation is organized as follows:

Chapter 2 reviews the concept of Inversion Coefficient and how it relates to the MOSFET I-V response. This chapter also reviews the MOS technology current and transconductance efficiency concepts. The relationship of the design variables to the inversion coefficient and the MOS Operating Plane are also discussed.

In Chapter 3 a new method to determine the technology current is developed. Using this new method is methodically repeated to perform a study of how the technology current value is affected by drain to source DC voltage, channel length and process variability via process corners. The concept of transconductance efficiency universality is confirmed. Our methods for measuring the MOSFET transconductance and output resistance parameters are further improved with the aid of Y-parameters measurements that help reduce the number of analyses and measurements needed to characterize the MOS process.

Chapter 4 uses the MOS characterization to develop design methodologies for the basic CMOS amplifiers, namely the NMOS common source with PMOS current load and the NMOS cascode with PMOS current load amplifier. The design methods are based on the transconductance efficiency and the current normalized output conductance of the MOS devices. Using an extension to the Y-parameters characterization technique it is

shown how to deal with the NMOS transistor in the presence of bulk effect. This chapter shows how well our method predicts the gain of these amplifiers by confirming the results with a simulation of the final design. The usefulness of the MOS operating plane for analog CMOS design of these basic amplifiers is also shown via the design tradeoffs of these amplifiers versus inversion coefficient and channel length studies.

Chapter 5 deals with the design of differential amplifiers and cascode (aka telescopic amplifier) differential amplifiers. The techniques developed deal with both the differential gain and common mode gain. The usefulness of the MOS operating plane for the design of these differential amplifiers is also shown via design tradeoffs of these amplifiers versus inversion coefficient and channel length studies.

Chapter 6 develops design techniques for the design of a simple OTA (operational transconductance amplifier). Several design choices are studied, such as zero DC offset and increasing of the OTA transconductance by increasing the current ratio of the current mirror all done at the design stage. The optimization of the performance of the simple OTA is performed and the results are compared to those obtained by Binkley, et al.

Chapter 7 summarizes the results of this dissertation and suggestions for possible future work are discussed.

# 2.0 BACKGROUND CONCEPTS

## 2.1 MOS IV response

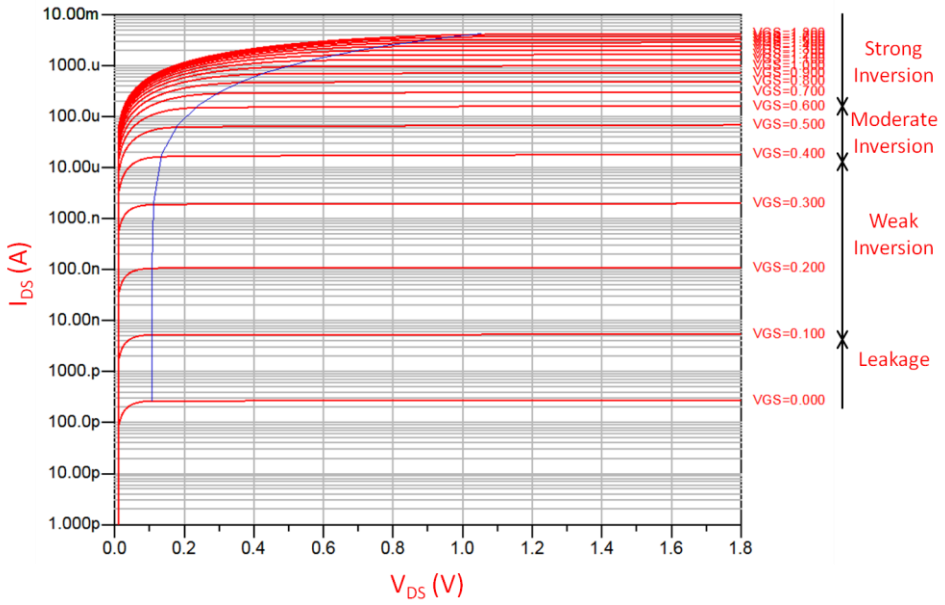
Looking at the transistor DC curves in Figure 2-1 three distinct regions can be identified [12]:

- Weak inversion
- Moderate inversion
- Strong inversion

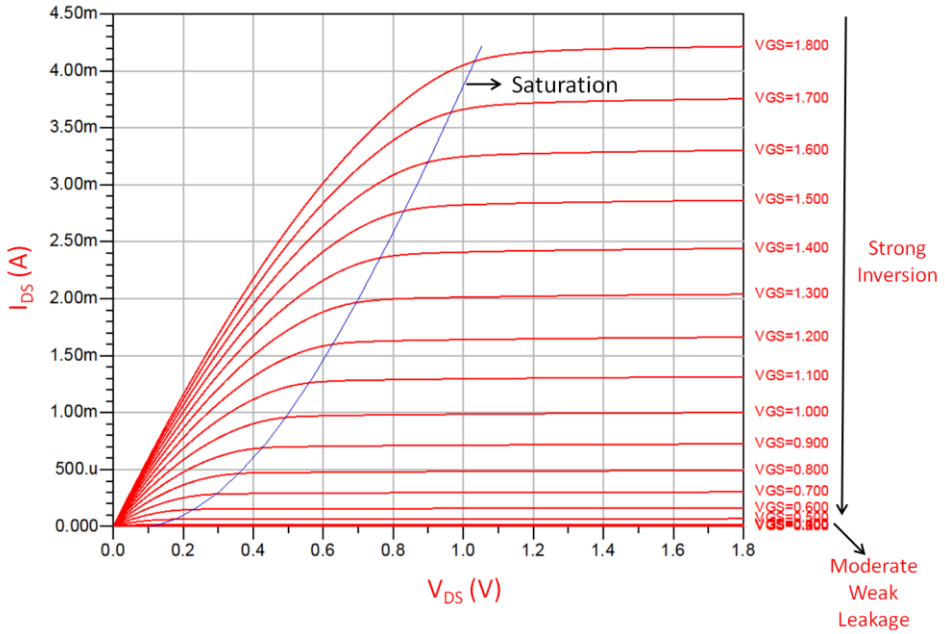
In the weak inversion region current is due to diffusion of carriers. The spacing on the curves is almost constant for fixed increments of $V_{GS}$. Since figure 2-1a is a log plot, $I_{DS}$ is exponentially related to $V_{GS}$ in this region. This is reminiscent of the bipolar transistor behavior in which the collector current is exponentially dependent on the base-emitter voltage. Typically $V_{GS}$ only varies a few tenths of volts in this region but the current can vary three to four orders of magnitude due to the exponential dependence on $V_{GS}$.

Current in the strong inversion region is due to drift. The spacing on the curves of figure 2-1b are proportional to the square of the effective voltage ($V_{eff}=V_{GS}-V_{TH}$). The drain current is approximately quadratic in $V_{GS}$. On this graph one can verify that $I_{DS}\approx k(V_{GS}-V_{TH})^2$.

In the moderate inversion region current is due to both drift and diffusion. The drain to source current ($I_{DS}$) is neither exponential nor polynomial function of $V_{GS}$ in this




(a)




(b)

Figure 2-1 $I_{DS}$ vs $V_{DS}$ for a Towerjazz CA18HB NMOS Transistor L=5 µm, W/L=20 and $V_{SB}$=0V. (a) $I_{DS}$ Logarithmic scale (b) Linear $I_{DS}$ scale

region. Transistor behavior changes gradually from exponential dependence on $V_{GS}$ to quadratic dependence on $V_{GS}$. In this region $V_{GS}$ varies a few tenth of a volt but the current can vary several orders of magnitude as seen in Figure 2-1a. Figure 2-1 also shows the gate leakage area of the response. Gate leakage is a small gate current when the transistor is in cutoff mode and is beyond the scope of this dissertation.

## 2.2 Inversion Coefficient

The degree of MOS channel inversion is quantified using the inversion coefficient (IC). An inversion level of one (IC=1) corresponds to the center of the moderate inversion region [1, 2]. The inversion coefficient is defined [3] in terms of the DC drain current of the MOS device, the shape factor (W/L) and the process technology current $I_0$, as follows:

$$IC = \frac{I_D}{I_0\left(\frac{W}{L}\right)} \tag{2.1}$$

where $I_D$ is the MOS drain quiescent current, W is the MOS channel width, and L is the channel length. In this thesis we frequently refer to the ratio W/L as the aspect ratio of the MOS transistor.

For a unity aspect ratio $I_0$ equals the DC drain current at what is known as the "center of the MOSFET moderate inversion region" [2] where IC = 1. Such a center is first defined by intersecting two well understood behaviors of the graph of $g_m/I_D$ vs. $I_D$, one that is constant for the weak inversion region and the other that obeys a square law for strong inversion. The latter is taken under the assumption of a long channel. In [3] that intersection solution is derived to be equal to:

$$I_0' = 2n\mu C_{OX} U_T^2 \tag{2.2}$$

where μ is the surface carrier mobility, n is the voltage division ratio between the gate oxide capacitor and the substrate depletion MOS capacitor, $C_{OX}$ is the gate oxide capacitance per unit area, and $U_T$=kT/q is the thermal voltage.

Note that $I_0$' is not constant, as both n and μ are bias-dependent and technology-dependent. The value of n can be determined from the slope factor n that is a function of the gate voltage [33]:

$$n(V_G) = \frac{1}{1 - \frac{\gamma}{2\sqrt{V_G - V_{TH} + \left(\frac{\gamma}{2} + \sqrt{\psi_0}\right)^2}}} \tag{2.3}$$

where $\psi_0$ is the surface potential, $\gamma$ is the substrate factor (aka body effect factor) ,and $V_{TH}$ is the threshold voltage. An approximation for n is presented in [6]:

$$n(V_G) \approx 1 + \frac{g_{mb}}{g_m} \tag{2.4}$$

In [3] a constant technology current $I_0$ is defined as:

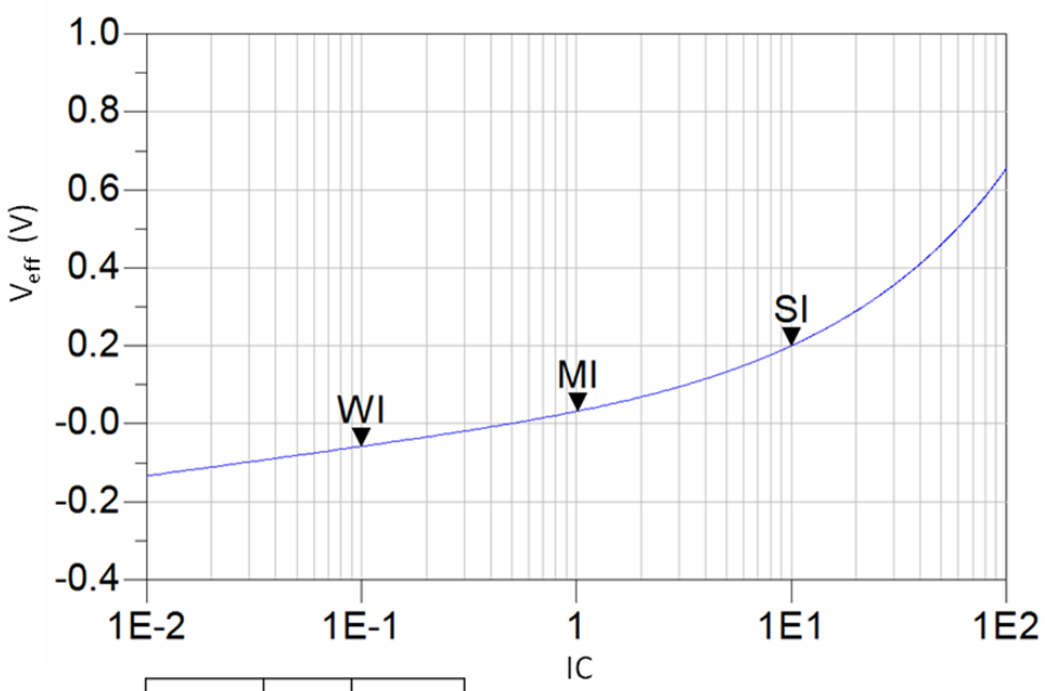
$$I_0 = 2n_0\mu_0 C_{OX} U_T^2 \tag{2.5}$$

where $\mu_0$ is taken according to the surface carrier mobility that is held fixed at its low-field value and $n_0$ is the voltage division ratio between the gate oxide capacitor and the substrate depletion MOS capacitor that is held fixed at its average value in moderate inversion. The value of $n_0$ is then determined either by evaluating (2.3) in the middle of the transistor moderate inversion region or by measurements of the bulk transconductance ($g_{mb}$) and of the transconductance ($g_m$) in the middle of the moderate inversion region followed by an evaluation of (2.4).

In the transconductance efficiency design method the effective voltage has been replaced by the inversion coefficient. The effective voltage $V_{eff}$ is given by:

$$V_{eff} = V_{GS}-V_{TH} \quad (2.6)$$

where $V_{TH}$ is the MOS threshold voltage. The relationship between IC and $V_{eff}$ can be easily determined via simulation and such a relationship is shown in Figure 2-2. The effective voltage is a complicated function of IC and is dependent on channel length once velocity saturation effects begin to occur at higher levels of inversion especially for short




| Marker | IC | $V_{eff}$ (V) |
|---|---|---|
| WI | 0.01 | -0.058 |
| MI | 1.0 | 0.032 |
| SI | 10.0 | 0.200 |

Figure 2-2 Effective voltage ($V_{eff}$) vs. Inversion Coefficient (IC) for a TowerJazz CA18HB process NMOS transistor $V_{DS}$=1.8V, L=4 µm and W/L=1

channel devices [3]. The weak inversion region occurs for an inversion coefficient IC<0.1, moderate inversion occurs for 0.1<IC<10, and strong inversion IC>10. The table with the marker information in Figure 2-2 indicates the $V_{eff}$ voltages for the high side of the weak inversion, the middle of the moderate inversion (IC=1), and the low side of the strong inversion. The results shown in Figure 2-2 are in good agreement with those published in [3]. An advantage of using IC instead of $V_{eff}$ for CMOS design is that IC is linearly related to the MOS transistor drain current ($I_D$) as seen from equation (2.1). This will uniquely define the value of channel width (W) needed once the other parameters of equation (2.1) become known.

## 2.3 MOS Drain Current

Weak inversion occurs for MOSFET operating at sufficiently low effective voltages. The Effective voltage vs. Inversion Coefficient of Figure 2.2 indicates $V_{Eff}$ = -56 mV is the weak inversion borderline (i.e. IC=0.1) for the TowerJazz CA18HB process. In the weak inversion region the channel is considered weakly inverted and the drain diffusion current dominates. The saturated MOS drain current is proportional in this region to the exponential of the effective gate to source voltage. Weak inversion drain current is approximated from the EKV model [6, 33] by:

$$I_{D,WI} = 2n\mu C_{OX} U_T^2 \left(\frac{W}{L}\right)\left(e^{\frac{V_{GS}-V_{TH}}{nU_T}}\right) \tag{2.7}$$

Strong inversion occurs for MOSFET transistors operating at sufficiently high effective voltages. Figure 2.2 indicates $V_{Eff}$ = 200 mV is the strong inversion borderline (i.e. IC=10) for the TowerJazz CA18HB process. In this region the channel is strongly

inverted and drain drift current dominates. Strong inversion drain current, excluding small geometry effects such as velocity saturation, is proportional to the square of the effective voltage. The strong inversion saturate MOS current is approximated by the EKV model [6, 33] by:

$$I_{D,SI} = \frac{1}{2}\left(\frac{\mu C_{OX}}{n}\right)\left(\frac{W}{L}\right)\left(V_{GS} - V_{TH}\right)^2 \tag{2.8}$$

Drain current in (2.7) and (2.8) is given for a MOSFET in saturation where $V_{DS}$ is greater than its saturation value (i.e. $V_{DS} > V_{DS,sat}$). The drain to source saturation voltage ($V_{DS,sat}$) is frequently taken as $V_{DS,sat} \approx (V_{GS} - V_{TH})$ while $V_{DS,sat} \approx (V_{GS} - V_{TH})/n$ is a better choice since the body effect along the channel raises the local threshold voltage and lowers the drain to source voltage required for channel pinch-off [6].

An expression for the entire inversion coefficient continuum is needed because equation (2.7) works well only in weak inversion and equation (2.8) works well in strong inversion. Both of these equations fail to determine the drain current in moderate inversion (i.e. $0.1 \leq IC \leq 10$). Using the EKV model [33] an all regions current expression is determined using interpolation function:

$$F(V) = \left[\ln\left(1 + e^{v/2}\right)\right]^2 \tag{2.9}$$

The resulting expression for the drain current [6, 33] is:

$$I_{D,all} = 2n\mu C_{OX} U_T^2 \left(\frac{W}{L}\right)\left[\ln\left(1 + e^{\frac{V_{GS}-V_{TH}}{2nU_T}}\right)\right]^2 \tag{2.10}$$

Using values for a 0.18 µm process provided in [6] we evaluated equations (2.8), (2.9) and (2.10) and plotted them in Figure 2-3. The process parameter values used to evaluate the current are shown on the figure. From the graph it is clear that (2.10) is acceptable in

all regions since it matches the weak and strong inversion region expressions very well and provides the drain current in the transition region (i.e. moderate inversion region).

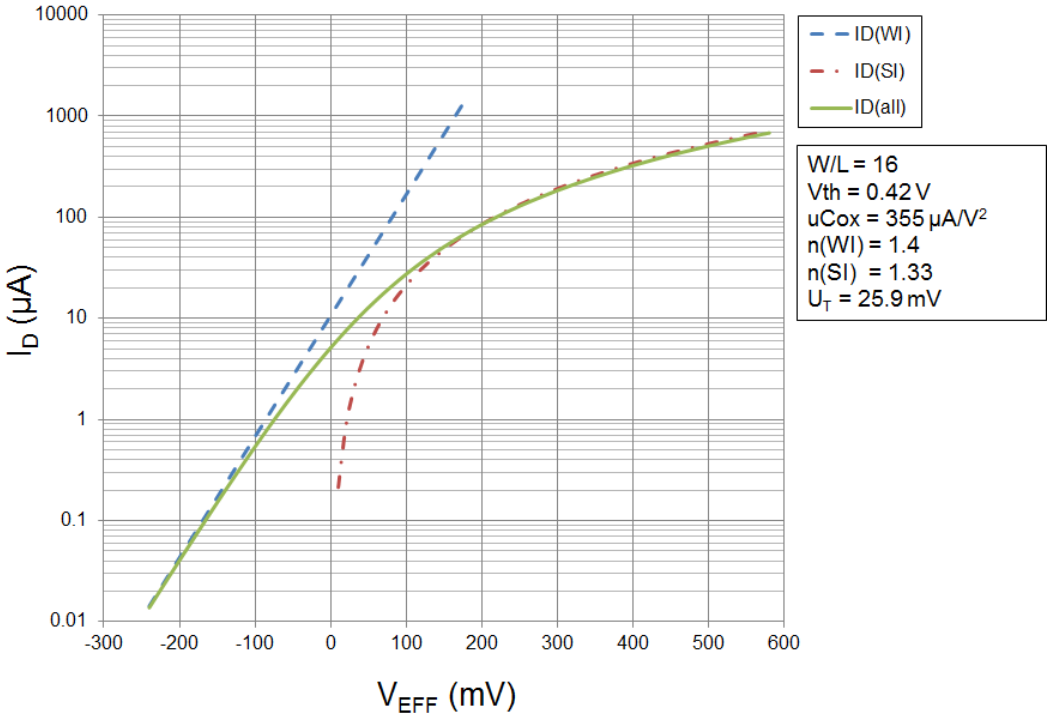



Figure 2-3 Drain Current versus effective voltage using weak, strong and all regions expressions.

A relationship between the technology current and the all-region current expression is possible by substituting (2.2) in (2.10):

$$\frac{I_{D,all}}{I_0^{'}} = \left(\frac{W}{L}\right)\left[\ln\left(1+e^{\frac{V_{GS}-V_{TH}}{2nU_T}}\right)\right]^2 \qquad (2.11)$$

## 2.4 Transconductance Effciency ($g_m/I_D$)

Modern analog designs methodologies utilize MOSFET transconductance efficiency $g_m/I_D$ measurements [3, 5, 7, 18 - 21]. The design methodology is based on the universal shape of the transconductance efficiency ($g_m/I_D$) vs. IC response [3, 7]; a graph of such a

response is shown in Figure 2-4. The limits of the MOS transconductance efficiency behavior are defined by two asymptotes (i) weak inversion asymptote and (ii) square law asymptote. The weak inversion asymptote approaches the thermal limit of the $g_m/I_D$ response [2]. The strong inversion asymptote approaches the square law region of the $g_m/I_D$ response [2]. The square law region will have a slope of -1/2 which is a result of the MOS transistor square law current region. The reader is advised that the square law behavior mentioned above is for a sufficiently long channel device (e.g. L=4 µm was used for Figure 2-3), we will study the implication of small channel length in chapter 3 of this dissertation. Under the assumption of a long channel behavior the weak inversion asymptote and the strong inversion asymptote intersect at the middle of the moderate inversion region (IC=1) [2] at a drain current that is exactly equal to the technology current.

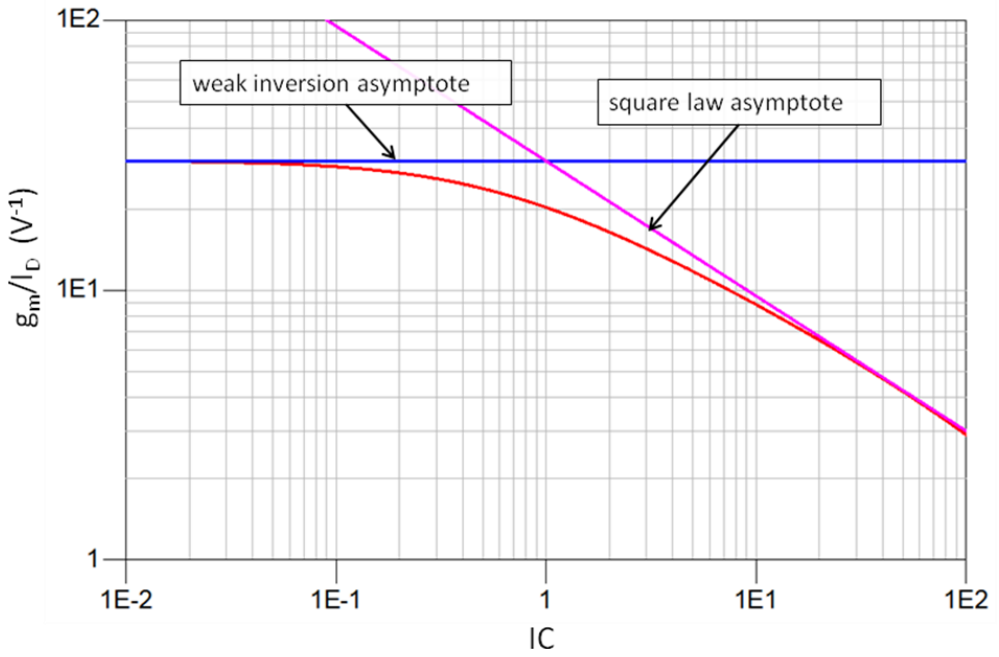



Figure 2-4 Transconductance Effciency vs. inversion coefficient (IC) for a TowerJazz CA18HB process NMOS transistor $V_{DS}$=1.8V, L=4 µm and W/L=1

## 2.5 CMOS Drain to Source Conductance and Early Voltage

A very important MOS transistor parameter needed for analog circuit design is the drain to source conductance ($g_{ds}$) and its relationship to the Early Voltage. In chapter 3 we noticed that only the level of IC determines the value of $g_m/I_D$. The drain to source conductance (or its reciprocal the drain to source resistance $r_{ds}$) is mainly controlled by the channel length (L). As is well known even from Level 1 MOS transistor models, the increase of $V_{DS}$ causes the channel pinch-off point to move towards the source. This results in an effective shortening of the channel length L and consequently in an increase of $I_D$. This current increase can be modeled by $r_{ds}$ if the same model hold on to the original drawn value of L. We clarify that over a small $V_{DS}$ voltage range around the bias point the increase in drain to source current is modeled as a fixed, small signal resistance $r_{ds}$ or conductance ($g_{ds}$) between the drain and the source. This drain to source small-signal model resistance can in Level 1 models be modeled using BJT-like Early Voltage ($V_A$) as $r_{ds}=V_A/I_D$. The increase in MOS drain to source current with $V_{DS}$ is modeled by the multiplicative correction term $1+V_{DS}/V_A$ multiplied by $I_{DS}$ that has no $V_{DS}$ dependency, as given by [7]:

$$I_{DS} = \left(I_{DS}\ \text{without}\ V_{DS}\ \text{dependency}\right) * \left(1 + \frac{V_{DS}}{V_A}\right) \tag{2.12}$$

In transistor technologies for which Level 1 models are no longer valid the MOSFET Early Voltage can no longer be considered constant. Early Voltage corresponds to a tangent line that touches the bias point on the $I_{DS}$ vs. $V_{DS}$ transistor curve. The slope of the tangent line on this curve is the drain to source conductance at this bias point. This slope or $g_{ds}$ is given by [7]:

$$g_{ds} = \frac{1}{r_{ds}} = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{I_{DS}}{V_{DS} + V_A} \approx \frac{I_{DS}}{V_A} \tag{2.13}$$

Often the effect of $V_{DS}$ on MOSFET small signal parameters is neglected. $V_A$ is a performance factor for MOSFETs that determines the value of $g_{ds}$ for a specified $I_{DS}$. Similar to $g_m/I_D$ that must be maximized to maximize $g_m$, $V_A$ should be maximized to minimize $g_{ds}$ (or equivalently to maximize $r_{ds}$ ). Early Voltage is a current normalized measure of $g_{ds}$ and it cannot be assumed fixed as is done for bipolar transistors. $V_A$ actually increases with channel length (L) and drain to source voltage ($V_{DS}$) [7]. In general $V_A$ will increase slightly with the level of inversion (IC) but this effect is rather secondary at best. The determination of $g_{ds}/I_D = (V_A)^{-1}$ can be done using the Y-parameters method discussed in section 3.5 and by using equation (3.4b). In Figure 2-6 we present the Early voltage curves for a TowerJazz CA18HB NMOS transistor for $V_{DS}=V_{GS}$ and L=0.25µm and W/L=10.

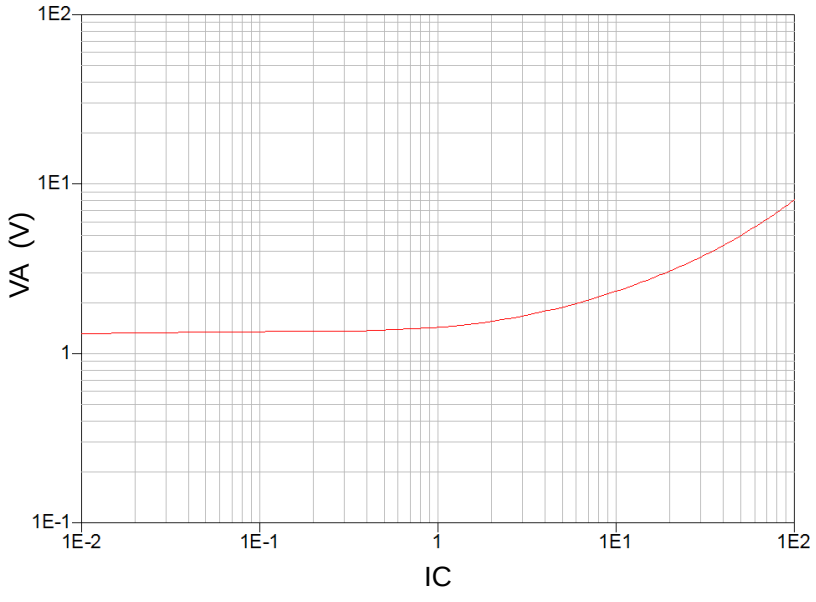



Figure 2-5 NMOS Early Voltage for TowerJazz CA18HB Process $V_{DS}=V_{GS}$ W/L=10, and L=0.25µm

## 2.6 Design Parameters and the MOS Operating Plane

For a MOSFET operating at a given drain current $I_D$ in saturation mode, the tradeoffs in circuit performance may be illustrated by a plane having the inversion coefficient and channel length as axes, these are the independent degrees of freedom in MOS design used in the $g_m/I_D$ design methodology. This plane is referred to in the literature as the MOSFET Operating Plane [3, 7]. Any MOSFET (in saturation) can be described by a point on the plane located by its selected MOS inversion coefficient and channel length. Different devices will likely operate at different locations on the plane as needed for different transconductance, output conductance, gain, bandwidth, and other design specification. In this thesis we use the MOS operating plane as a qualitative guidance whether to raise or lower the IC and L values for the MOSFETs in a given circuit design. The width (W) of the MOS transistor is determined by the selected IC value using (2.1). In order to determine the value of $V_{GS}$ (gate to source voltage) one needs to know the relationship between IC and $V_{GS}$ which is obtained via simulation or measurement.

The design of any fundamental analog circuit also requires knowledge of the current normalized conductances ($g_{ds}/I_D$) vs. IC relationship. Current normalized conductances are needed along with the transconductance efficiency to calculate such quantities as the small-signal voltage gain of the amplifier being designed. The $g_{ds}/I_D$ values are determined via measurements or basic AC simulation. In this research AC analysis is performed at a low enough frequency such that the internal MOSFET transistor capacitors are essentially negligible and a DC analysis allows for the measurement of the quiescent drain current.

Using the MOS Operating Plane a designer can easily establish multiple observations such as:

a) That MOS capacitances and intrinsic-gain bandwidth are optimized at high inversion coefficient level and minimum channel length.

b) Conversely, MOS intrinsic gain, DC matching, and gate-referred flicker-noise voltage are optimized for low inversion coefficient and maximum channel length.

c) Drain–source saturation voltage, transconductance, and gate-referred white-noise are optimized at low inversion coefficient.

d) Transconductance linearity is optimized at high inversion coefficient.

e) Output resistance is optimized at maximum channel length.

These performance tradeoffs and their management for optimal analog CMOS design are central to this design methodology and will be referred to throughout this research.

## 2.7 MOSFET Models and Design Kit Verification

The validation of MOSFET foundry models is a critical step for designers of CMOS analog circuits. Important parameters for the design procedures developed in our research are the transconductance efficiency ($g_m/I_D$) and the Early Voltage (VA). Designers should verify that these parameters are properly emulated by the models in the foundry design kit before proceeding to do any Analog CMOS circuit design. We provide a few guidelines of what to look for when working with foundry design kit models.

In order to verify the MOSFET models the designer should first determine the value of the technology current ($I_0$) as per the procedures discussed in chapter 3 of this

dissertation. Using the MOSFET characterization concepts discussed in section 4.4 will then allow the construction of the transconductance efficiency and current normalized output conductance curves that are critical to the analog CMOS design methods developed herein.

Let us now show what the proper response for the aforementioned quantities should look like and a few responses that do not meet the requirements. First we show the transconductance efficiency for a NMOS transistor L = 0.5 µm, W/L = 100 and $V_{DS}$ = $V_{GS}$ in Figure 2-6. This graph shows the response for the same device using BSIM3.1 and PSP models. Notice that the PSP trace matches the ideal results shown for a long channel

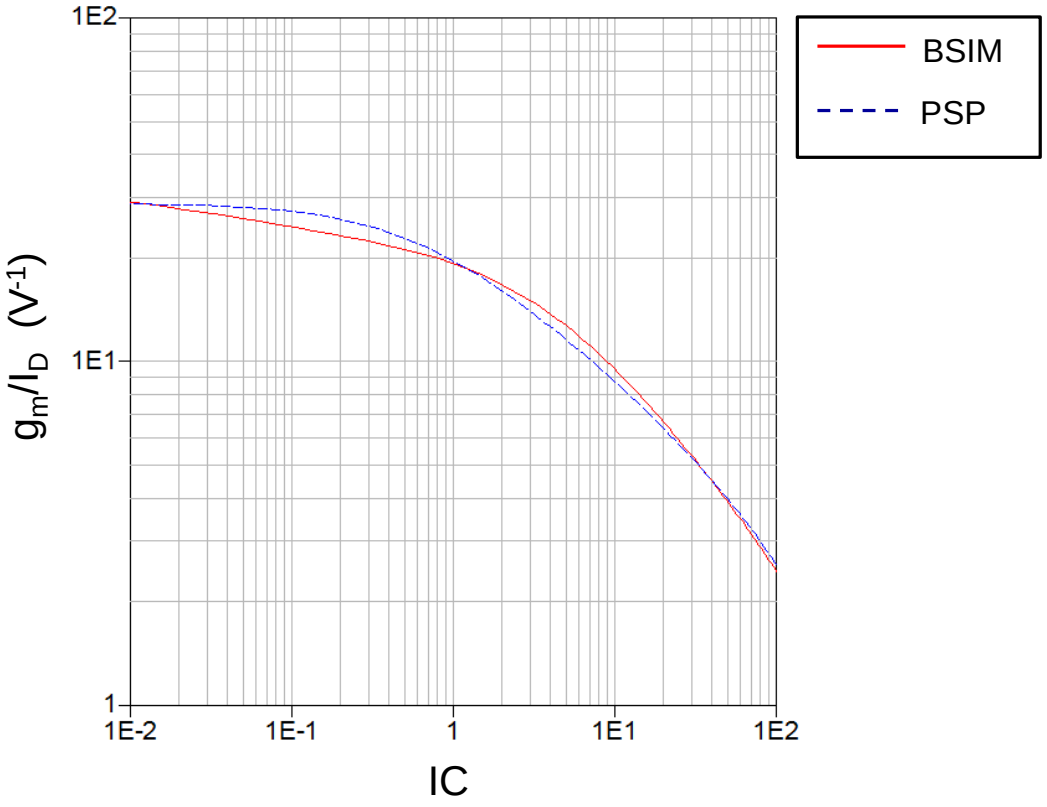



Figure 2-6 Comparison of Transconductance Efficiency for NMOS transistor L = 0.5 µm, W/L = 100 and $V_{DS}$ = $V_{GS}$

device as in Figure 2-3, i.e. it shows the graphs approaches the thermal limit in weak inversion and drops to approximately 70% of this value in the middle of moderate inversion (IC=1) and then continues to drop in strong inversion. Observing the BSIM trace we notice that in weak inversion it does not stay flat on the weak inversion region of the response and starts to drop faster than we expected. While looking at this graphs it does not seem to be more than a 10% difference such error can become cumulative when designing analog CMOS circuits with several transistors and will be an additive error in addition to the normal process variations.

Figure 2-7 shows a VA comparison between a BSIM3.1 and PSP model for a similar device as the one used for the transconductance efficiency study above. We note

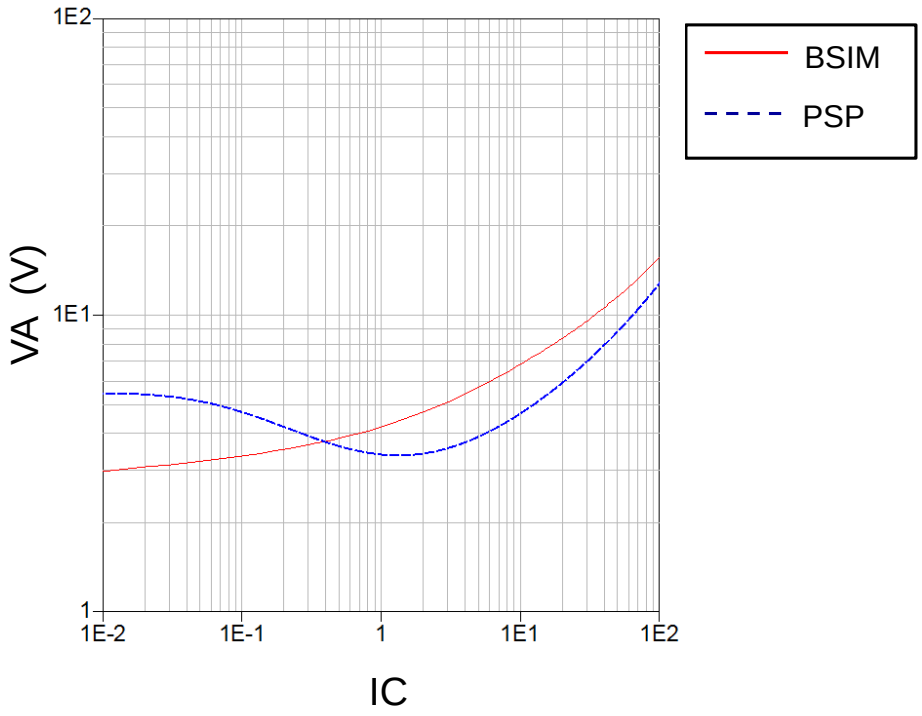



Figure 2-7 Early Voltage Simulated Results for NMOS transistor L = 0.5 µm, W/L = 100 and $V_{DS} = V_{GS}$

that the results for the BSIM model follow the same trend as those shown in Figure 2-4. Clearly we see that the VA value for the BSIM model is flat in weak inversion and increases as the device is biased in strong inversion. The issue in Figure 2-8 is actually with the PSP model results. Notice how the PSP model VA results drops in the moderate inversion elow the values in weak inversion. The errors shown in Figures 2-6 and 2-7 point to a possible problem with the model parameter extraction measurements and routine or possibly a fundamental model problem. The modeling of MOSFET transistors is beyond the scope of this dissertation and is considered as future research.

# 3.0 TECHNOLOGY CURRENT

## 3.1 Technology Current Determination Method

As implied by equation (2.1) for a unity aspect ratio $I_0$ equals the DC drain current at the center of the MOSFET moderate inversion region [2] where IC = 1. Given any MOSFET model obtained from a semiconductor foundry, the user can always set the aspect ratio W/L to 1, embed the transistor in a simulation test circuit containing a large enough and fixed DC source for $V_{DS}$ that guarantees saturation and a variable DC source for $V_{GS}$ and sweep $V_{GS}$ to obtain a plot of the transconductance efficiency curve $g_m/I_D$ vs. $I_D$. Whenever using such relationship that is based on actual data points the weak inversion horizontal asymptote can be extrapolated from the region where $g_m/I_D$ approaches the thermal voltage limit. The strong inversion asymptote on the other hand on a logarithmic scale, and under the assumption of no velocity saturation effects, has a slope of -1/2 representing the ideal "square law" region of the transconductance efficiency curve. The -1/2 slope is valid only for a sufficiently long device that does not exhibit velocity saturation or VFMR effects and as long as the MOSFET device is operating in saturation mode. The weak inversion and strong inversion asymptotes intersect at what is defined as the middle of the moderate inversion region (also defined as IC=1) at a drain current $I_D$ that equals exactly $I_0$.

Our research utilizes a graphical determination method for $I_0$. This graphical method of the determination of $I_0$ is done by iteratively intersecting the horizontal weak

inversion $g_m/I_D$ line with a candidate square-law strong inversion region asymptote line (that has a slope of -1/2 and an undetermined location).

In Figure 3-1 the procedure flowchart for the determination of $I_0$ is presented. The determination of $I_0$ starts with a unity aspect ratio device setup with a bias applied such that saturation is guaranteed and that no terminal voltage exceeds the foundry process maximum values. Drain current is measured while $V_{GS}$ is swept to a maximum voltage of interest. Calculation of the transconductance ($g_m$) and transconductance efficiency is performed and the $g_m/I_D$ vs. $I_D$ relation becomes known (see Figure 3-2). Selecting an initial value of $I_0$, while not a critical selection for this algorithm to work, could be done based on some a-priori reasonable estimates, for example in the experiment that produced Figure 3-2, 1 µA was used which places the initial strong inversion candidate line to the right of where the actual solution is expected. The weak inversion asymptote is a horizontal line that coincides with the maximum transconductance efficiency as mentioned previously this line intersects the strong inversion asymptote precisely at a drain current $I_D=I_0$. This defines a point on the strong inversion asymptote $[I_0,(g_m/I_D)_{max}]$ line. Since the slope and a point are known for the strong inversion asymptote the square law line (SQL) candidate is uniquely defined. Refer to Appendix A for the derivation of the SQL formula. The vertical distance between the SQL and the $g_m/I_D$ data is then determined by calculating the corresponding vertical value differences for each $I_D$. The minimum value of these differences is taken as the distance between the two curves. If the distance between the two curves is zero then the SQL line becomes a curvilinear tangent asymptote to the $g_m/I_D$ curve and thus $I_0$ has been determined.

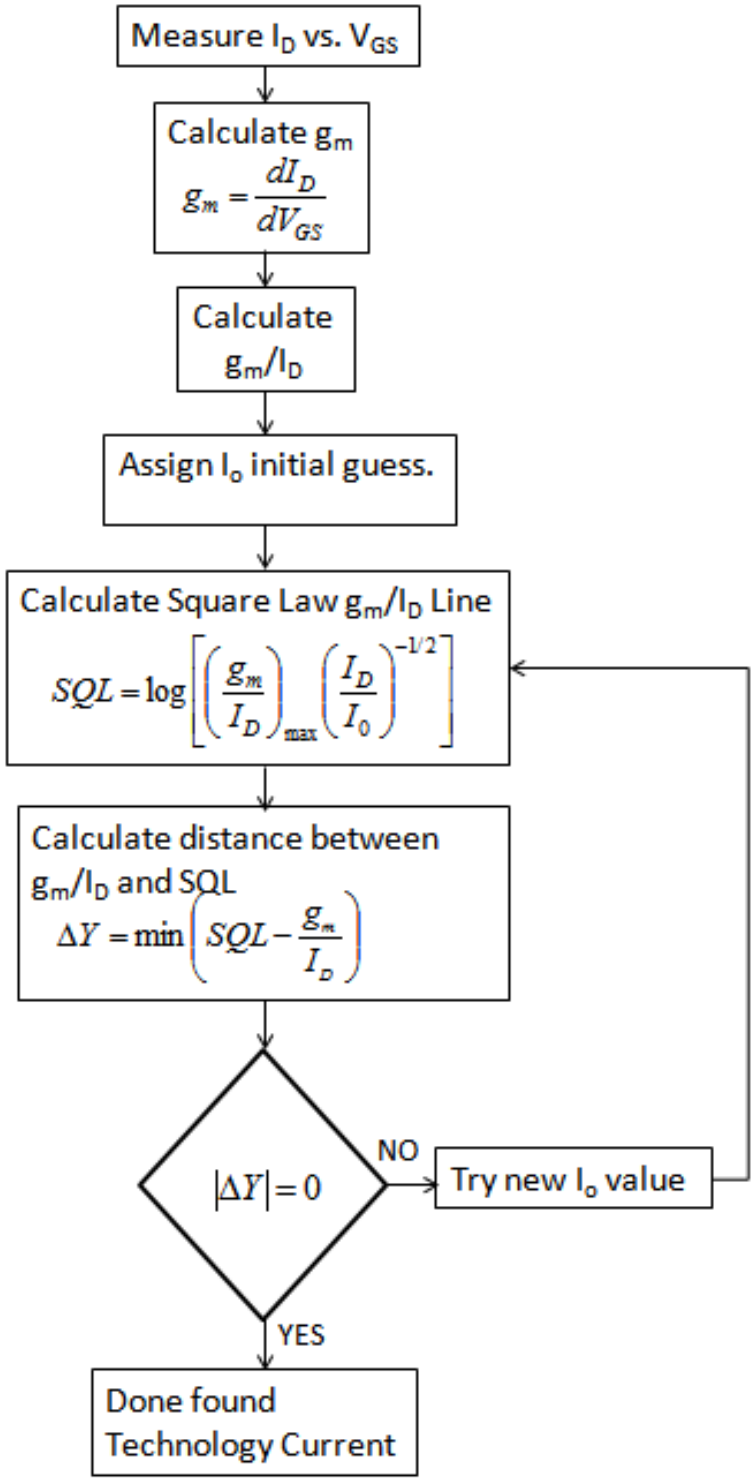



Figure 3-1 Technology Current ($I_0$) Determination Flowchart

The search for a unique correct square law line can be facilitated by any analog simulator optimizer software, in which the line X-intercept point is varied, and the termination criterion is set based on minimizing the distance between the straight-line candidate and the actual transconductance efficiency curve as function of $I_D$. For example, using ADS 2009 (by Agilent technologies Inc.), the simulation mode was set to DC, the optimized variable was set to $I_0$ and the optimization criterion was set to minimize the distance between the two curves as per the Figure 3-1 flowchart. If an optimizer is not available the user can manually vary $I_0$ until $|\Delta Y|=0$ (see Figure 3-3).

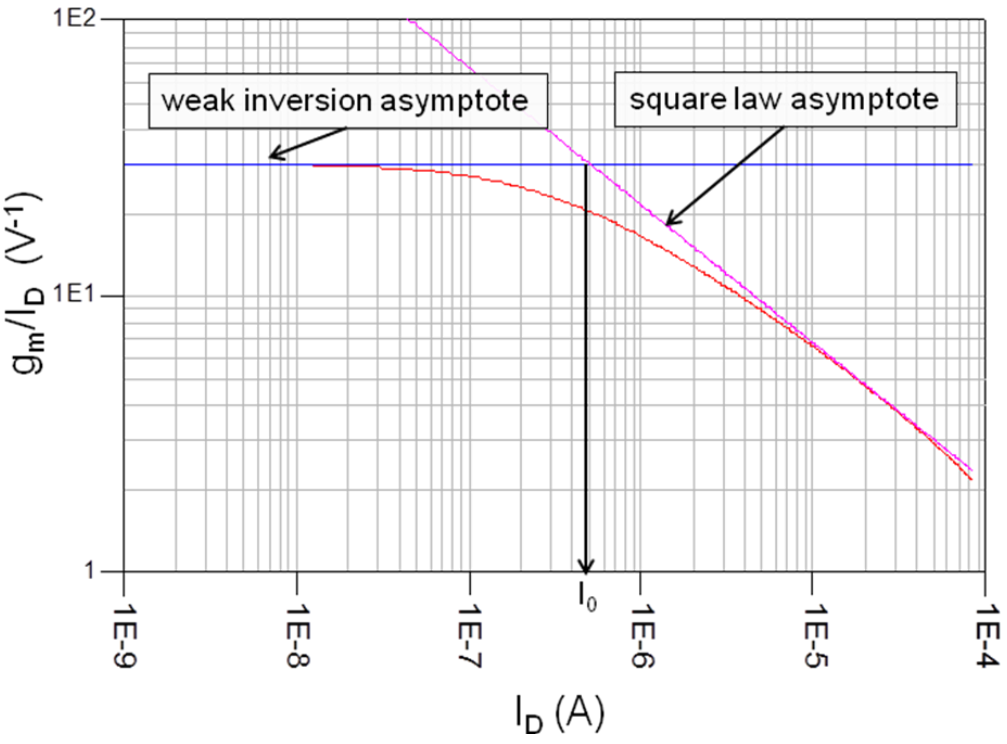



Figure 3-2 Transconductance Efficiency gm/ID vs. drain current for a TowerJazz NMOS transistor $V_{DS}$=1.8V. L=4 μm and W/L=1.

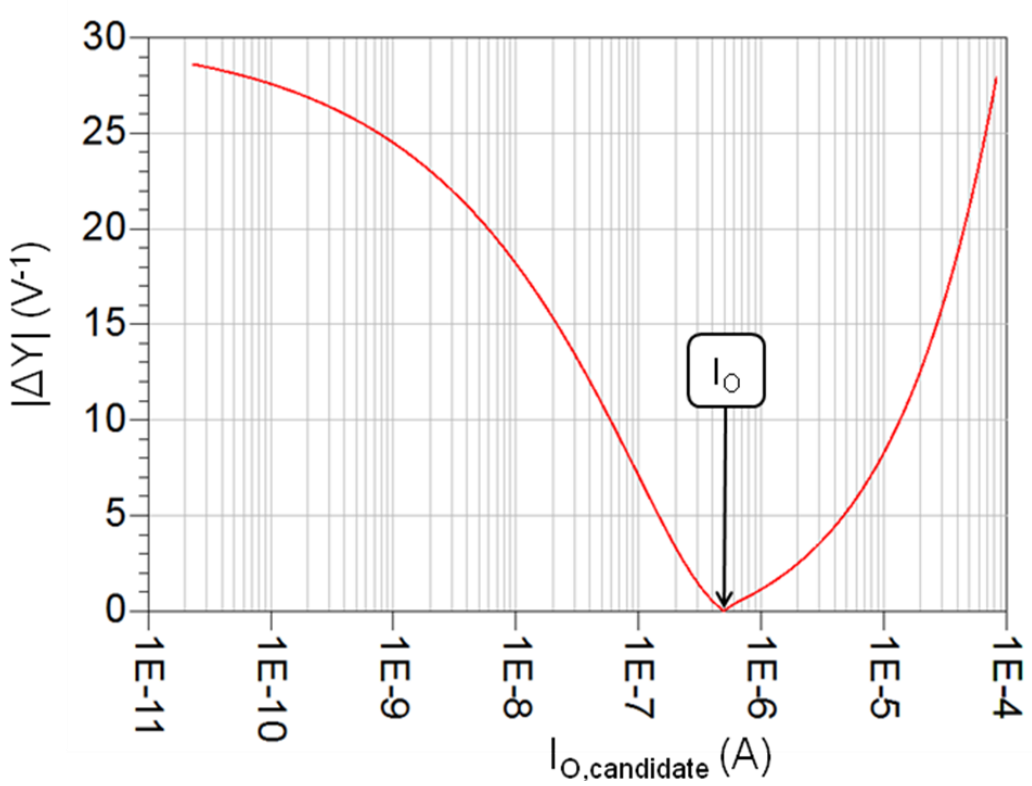



Figure 3-3 Magnitude of ΔY versus $I_0$ candidate values obtained for a TowerJazz CA18HB process NMOS transistor $V_{DS}$=1.8V, L=4 µm and W/L=1.

## 3.2 $I_0$ Determination - Direct Method

The implementation of the $I_0$ determination technique presented in Figure 3-1 was done using Advance Design System from Agilent Technologies, Inc. [13]. The version used is ADS2009 Update 1. Schematic and simulation setup to measure $I_{DS}$ vs. $V_{GS}$ is shown in Figure 3-4. The setup shown is for a NMOS transistor; the PMOS transistor is very similar and not shown. Notice that it is important to have a fine sweep of $V_{GS}$ in order to get enough samples to have accurate transconductance results since $g_m$ is going to be determined using numerical differentiation. In this thesis based on our experience a 1 mV sweep step size for $V_{GS}$ produces accurate results as shown in Figure 3-4.

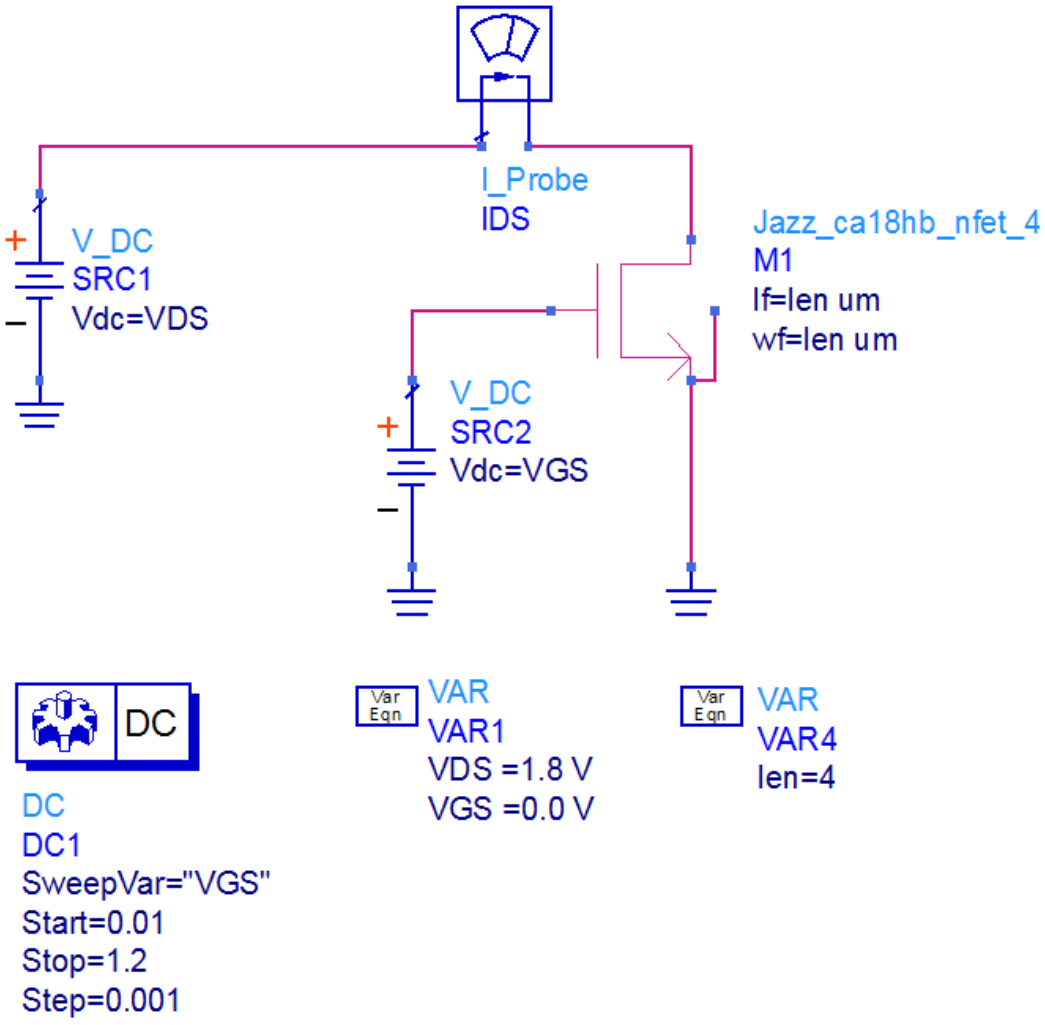



Figure 3-4 NMOS Technology Current Determination Simulation Setup using ADS

Once the simulation is run the results are then post-processed in the ADS data display window. Notice that the above simulation is available in any SPICE like simulator and therefore there is no special ADS feature needed to perform the $I_0$ determination method. The process does require some form of data processing as per our following discussion.

The calculation process required in other simulation tools may be different than what is required in ADS but should follow the steps delineated in the "Technology Current Determination Flowchart" shown in Figure 3-1. The equations shown in Figure 3-5 are the ADS implementation of the flowchart. In equation (1) the number of data points is determined. This value is needed because the numerical differentiation always produces a data array with one element less than the arrays of data points that serve as an input. Equation (2) actually sets up an array such that the current that is going to be used to calculate the transconductance efficiency vs. $I_D$ has the same number of points as the differentiated data array. In equation (3) of Figure 3-5 the differentiation of $I_D$ takes place as diff(IDS.i). We then divide this value which equals the transconductance ($g_m$) by the $I_D$ drain current data array to produce the transconductance efficiency value ($g_m/I_D$). Results as those shown in Figure 3-2 require a data array of $g_m/I_D$ vs. $I_D$ this is why we use the vs() function in equation (3).

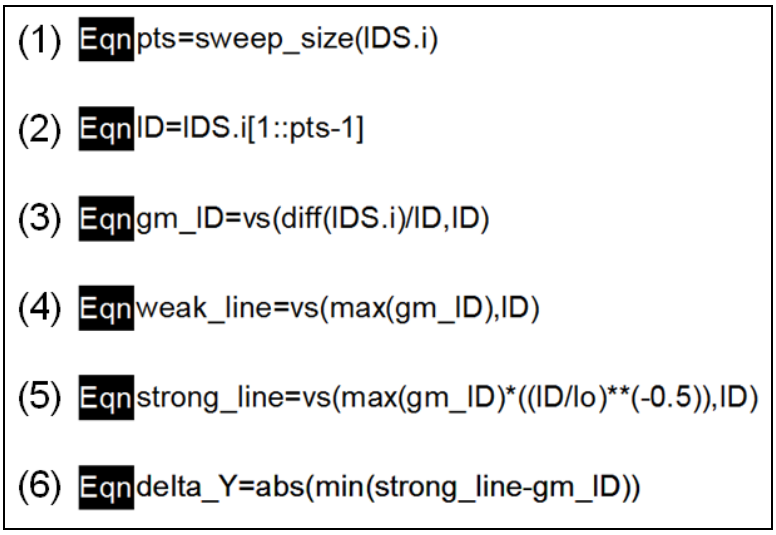



Figure 3-5 ADS Post-Processing for $I_0$ Determination Equations

The next step in the process requires the initialization of an $I_0$ candidate value or initial value. In accordance to the flowchart this value will need to change since it is only an initial estimate, we have decided to implement this search with an ADS slider as shown in Figure 3-6 so that we can easily implement the decision loop of the flowchart. Following the flowchart we then calculate the square law line (SQL) in equation (5) and $\Delta Y$ (i.e. distance between $g_m/I_D$ and SQL) in equation (6).

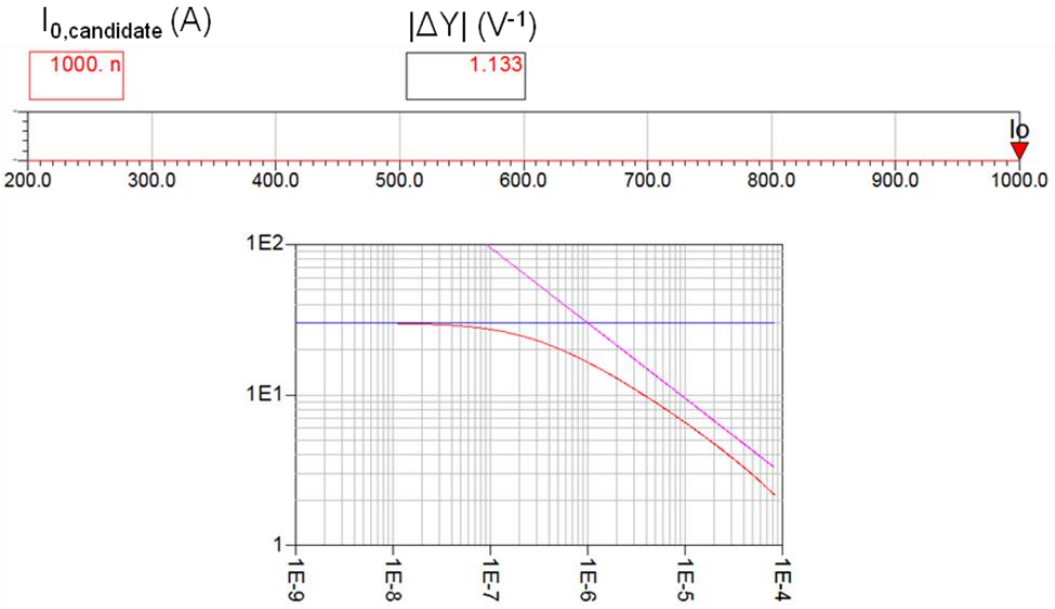



Figure 3-6 Slider being used to initialize $I_0$ candidate value

The initial value of $I_0$ was set to 1 µA as shown in Figure 3-6, this results in a $\Delta Y$=1.133 $V^{-1}$. This initial estimate is obviously not the value of zero that we would like; in fact it results in a SQL that is noticeably separated from the $g_m/I_D$ curve as shown in Figure 3-6. At this point in the flowchart we are at the decision junction and since $\Delta Y$ is not close enough to zero we must iterate around the loop which is accomplished by moving the slider shown in Figure 3-6 until $\Delta Y$ is zero or close enough for any practical purpose. The process of moving the slider continues until that value of $\Delta Y$ is reasonably

close to zero as shown in Figure 3-7 in which ΔY=0.001. Notice how in Figure 3.7 the SQL is tangential to the $g_m/I_D$ curve, i.e. $I_0$ has been determined to be 497 nA for the Jazz CA18HB NMOS transistor. Likewise $I_0$ of the Jazz CA18HB PMOS was determined to be 196 nA.

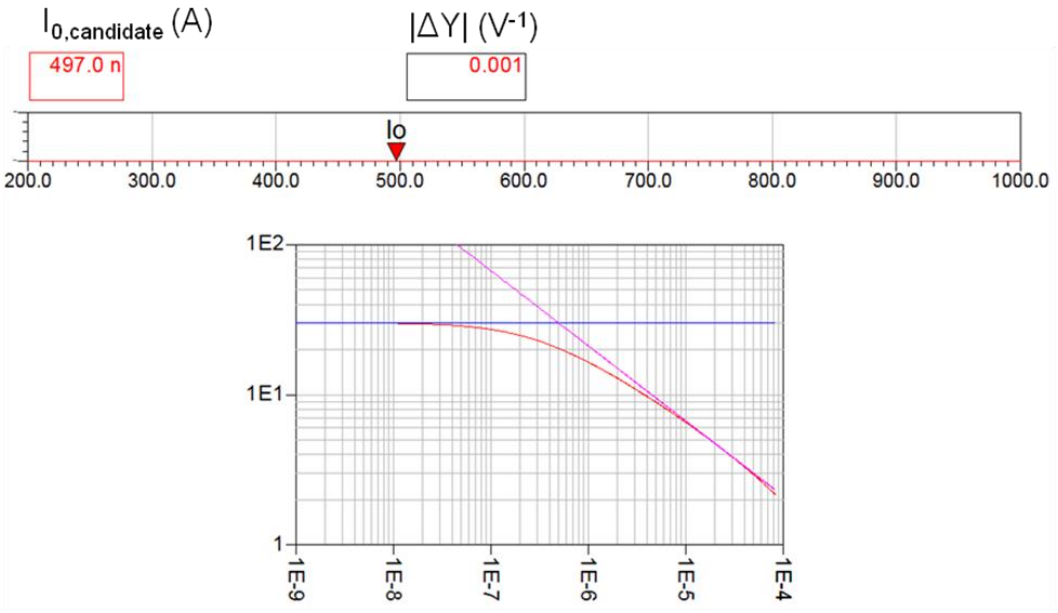



Figure 3-7 $I_0$ Value Determination Illustration

## 3.3 Process Corners, L and $V_{DS}$ effects and the Determination of $I_0$

The technology current is also process dependent, i.e. it will be different for the so called slow, nominal and fast MOS devices. These process corners depend on several chosen physical parameters like the oxide thickness ($t_{ox}$), channel doping, drain/source doping, technology (e.g. 0.18 um), reduction in channel length from its drawn value, threshold voltage, etc. The chosen physical testable parameters are deemed to represent the entire set of process parameter variations. Based on statistical analysis the ±3σ values of each physical parameter are first determined by the foundry. The 3σ-fast model is

found using either the +3σ or the -3σ of each parameter, depending which option yields a larger device current. For instance, for $t_{ox}$ the smaller extreme value is taken as part of the "fast corner" model. Likewise for the 3σ-slow parameters for NMOS and PMOS devices [5, chap 14].

The technique developed in section 3.2 allows the study of $I_0$ versus process corners. The technology current is expected to be bias conditions independent. In order to study whether or not $V_{DS}$ influences $I_0$ the process of estimating $I_0$ may be repeated as $V_{DS}$ is swept. The results of this analysis are shown in Fig. 3-8. A 0.18 μm process NMOS with L = 4 μm and with a shape factor of 1 was used. Note that the value of $I_0$ drops significantly for $V_{DS} < 0.5V$ because the device may no longer be in saturation mode as $V_{DS}$ is either close to $V_{Dsat}$ or even smaller than it.

The average error for the value of $I_0$ for $V_{DS} > 0.5V$ is approximately 2% (even for process corners) across the range of bias voltages of practical interest. We expect that the voltage after which the value of $I_0$ becomes fairly constant is process dependent. That is $I_0$ is a "special current" but still obeys basic MOS operation so it becomes nearly constant for $V_{DS} > V_{Dsat}$. As expected the value of $I_0$ is fairly insensitive to $V_{DS}$ as long as the MOS device is in saturation. A somewhat surprising observation is that the values of $I_0$ are quite sensitive to process corners. The $I_0$ value for a slow process is less than a nominal process with the fast process having the highest value. This can be intuitively deduced from equation (2.1) since a faster process has a smaller $t_{ox}$ which in turn means a larger value of $C_{ox}$ and hence a higher value of $I_0$.

From [2] the value of $I_0$ can be estimated from the intersection of the weak inversion asymptote and the strong inversion asymptotes as was shown in section 3-2. It is safe to say that for a "large enough" device one can use this technique to establish a single constant value for $I_0$ to be used in subsequent sub-micron analog design. Figure 3-9

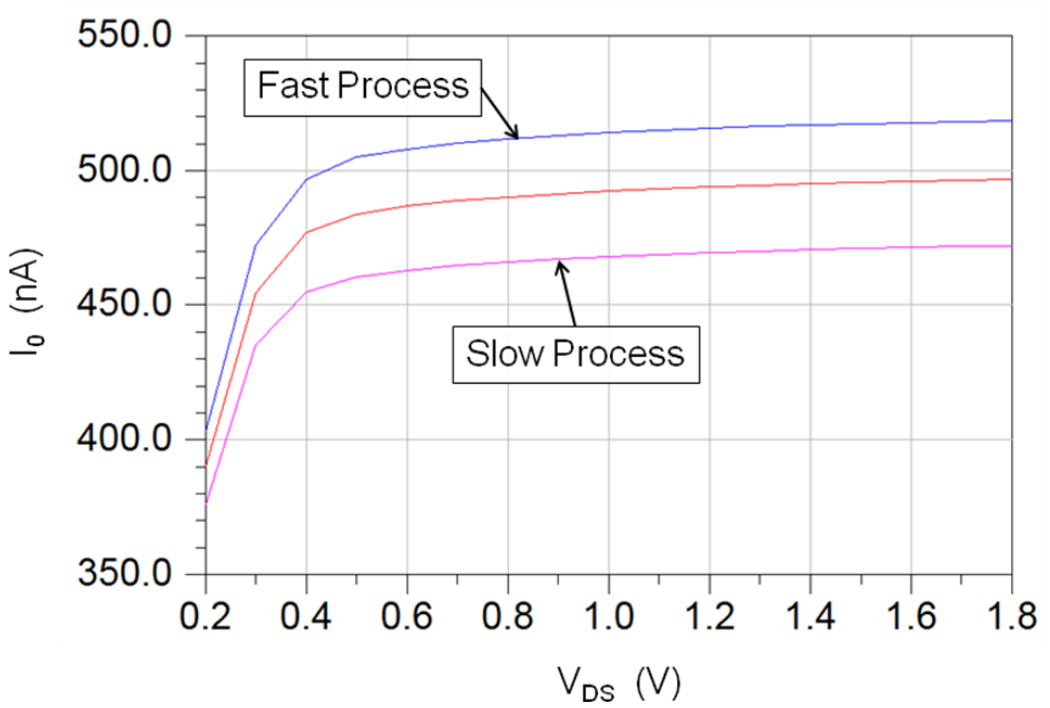
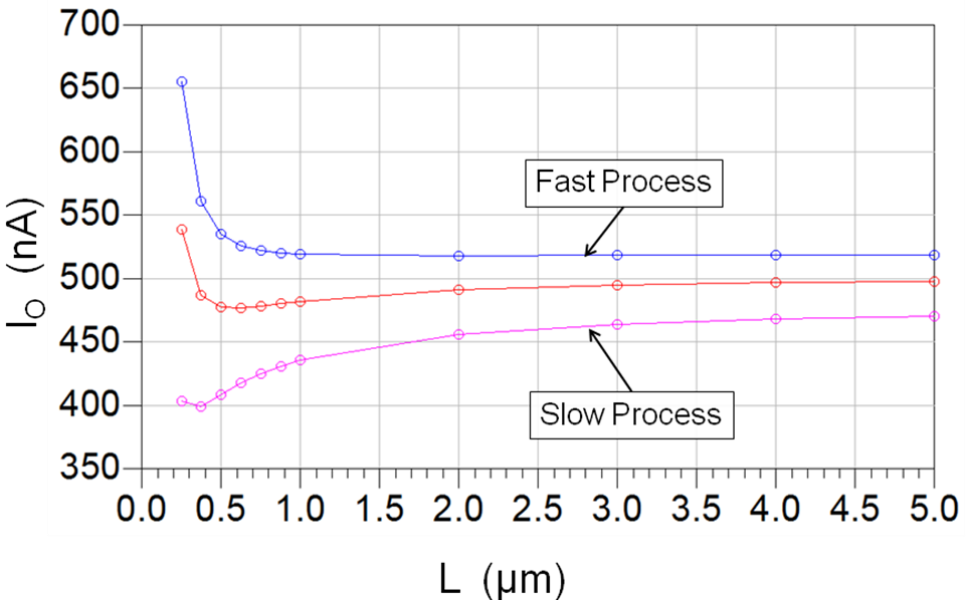



Figure 3-8 The identified $I_0$ vs. $V_{DS}$ and Process Corners for a TowerJazz NMOS Transistor L=4 um W/L=1.

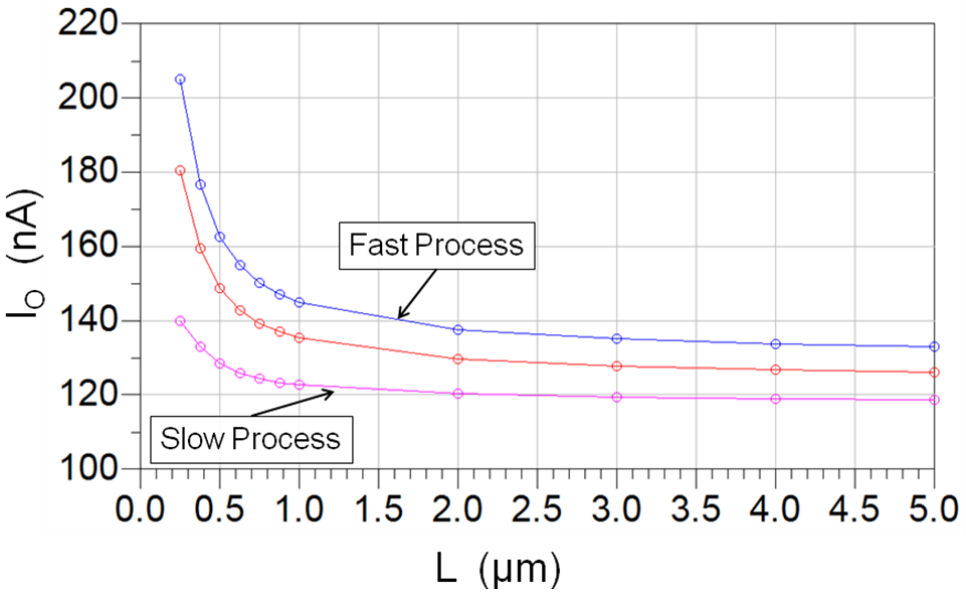
shows technology current estimation results as the channel length for a NMOS and a PMOS device (for $V_{DS}$ = 1.8V) is swept. The results show that using $L \geq 2$ µm is a good estimate for the minimum channel length at which $I_0$ is to be determined.

Analog designers often refer to the "universality" of the transconductance efficiency versus inversion coefficient curve. To check how sensitive is such a curve to process corners, $I_0$ estimated results, that take into account adjustments of $I_0$ due to process corners, have been utilized to draw three such curves, nominal ,fast and slow, as

shown in Figure 3-10. The results presented in Figure 3-10 substantiate the "universal" nature of the transconductance efficiency versus inversion coefficient curve as all three curves were shown to have very similar shapes.




**(a)**




**(b)**

Figure 3-9 $I_0$ vs. L and Process Corners for $V_{DS}$=1.8V (a) NMOS (b) PMOS

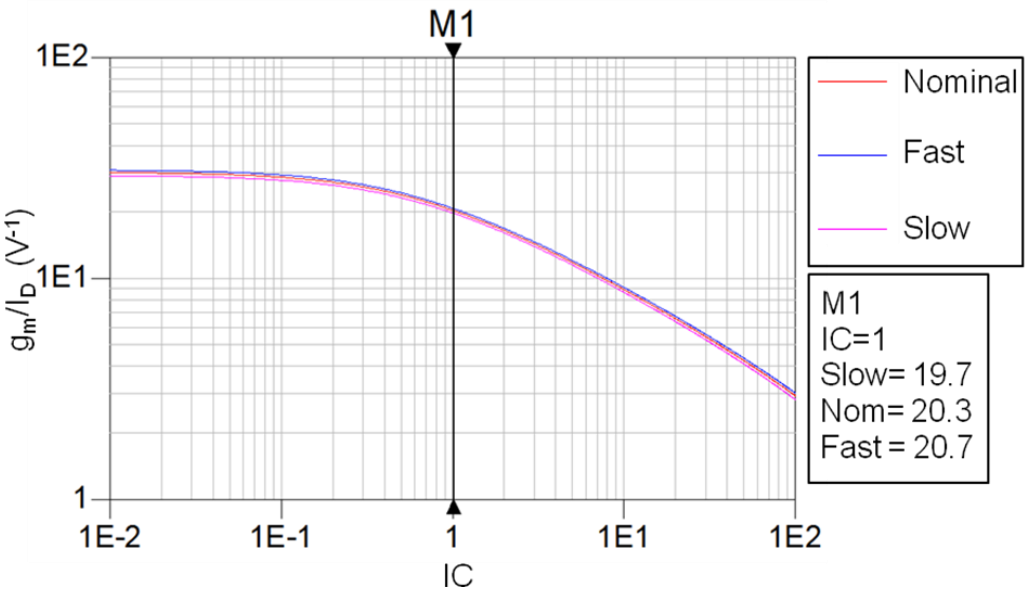



Figure 3-10 $g_m/I_D$ and Process Corners (L=4 um and $V_{DS}$=1.8V) using correct $I_0$ for each process corner

The transconductance efficiency versus inversion coefficient curves shown in Figure 3-11 are obtained from the identified $I_0$ values based only on the nominal MOS device. The results at the marker in Fig. 3-11 show that the $g_m/I_D$ value has a 1.5% error for the slow device and 0.95% error for the fast device if one uses the nominal $I_0$ value. In most design applications this is an acceptable error.

## 3.4 Y-parameters Method for the Determination of $g_m$ and $g_{ds}$

The manual $I_0$ determination procedure shown in section 3.2 is simple and can be implemented in any simulator and does not require any ADS advanced features. It can however be labor intensive especially for those analyses shown in section 3.3 in which many different conditions required repeated new determinations of $I_0$. In a laboratory setting this approach becomes very labor intensive and prone to operator error due to all

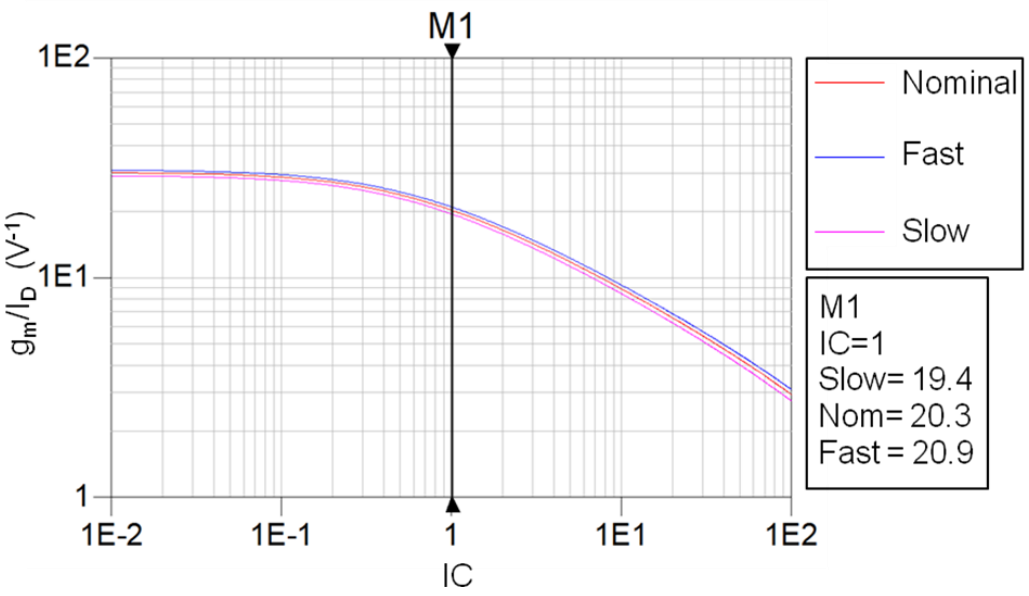



Figure 3-11 $g_m/I_D$ and Process Corners (L=4 um and $V_{DS}$=1.8V) using $I_0$ from Nominal Process.

the DC voltages and current measurements required. Whenever designing CMOS amplifier circuits a faster process to determine $g_m/I_D$ and $g_{ds}/I_D$ is needed. The solution to these challenges is to use two port Y-parameters to characterize the CMOS devices.

Y-parameters are described by two equations that relate the voltages and currents at the two ports as shown in Figure 3-12 and are given by:

$$I_1=Y_{11}V_1+Y_{12}V_2 \quad (3.1a)$$

$$I_2=Y_{21}V_1+Y_{22}V_2 \quad (3.1b)$$

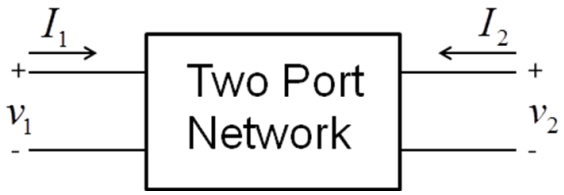



Figure 3-12 Linear Two Port Network

Y-parameters have units of admittance and are calculated by shorting one of the ports and measuring the currents as defined in Figure 3-12, that is:

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} \tag{3.2a}$$

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} \tag{3.2b}$$

$$Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0} \tag{3.2c}$$

$$Y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0} \tag{3.2d}$$

Y-parameters are determined for the MOS small signal equivalent circuit of a MOS transistor with the source and bulk grounded and can be used to determine the transconductance ($g_m$) and drain to source conductance ($g_{ds}$) of the MOS transistor. This is done by first calculating the Y-parameter based on Figure 3-13. The measurement of Y-parameter is done by shorting either $v_{gs}$ or $v_{ds}$ and measuring $i_{gs}$ and $i_{ds}$. Close examination of Figure 3-13 reveals that there are four unknowns, namely $y_{gs}$, $y_{gd}$, $g_m$, and $y_{ds}$.

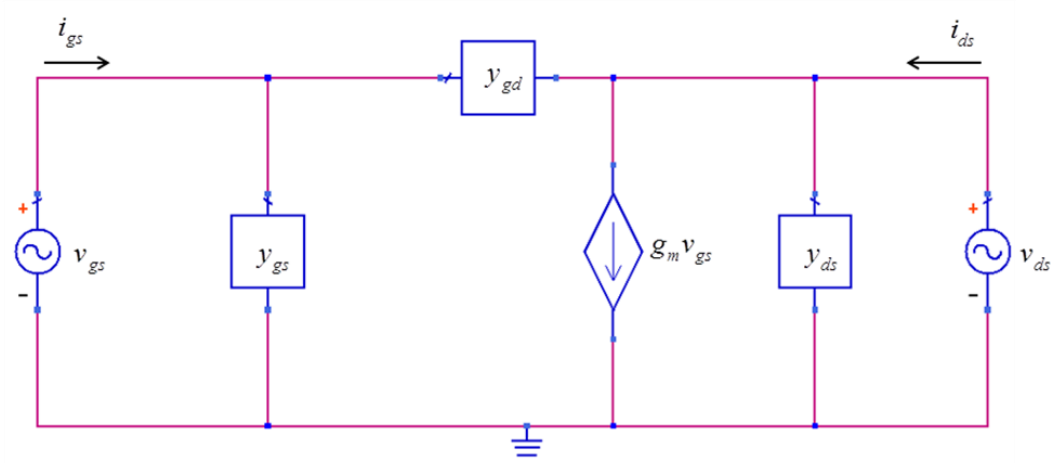



Figure 3-13 MOS Small Signal Equivalent Circuit referenced to the source

The simultaneous solution is as follows:

$$Y_{11} = y_{gs} + y_{gd} \tag{3.3a}$$

$$Y_{21} = g_m - y_{gd} \tag{3.3b}$$

$$Y_{12} = -y_{gd} \tag{3.3c}$$

$$Y_{22} = y_{gd} + y_{ds} \tag{3.3d}$$

From equations (3.3) the values for $g_m$ and $g_{ds}$ are:

$$g_m = real(Y_{21} - Y_{12}) \tag{3.4a}$$

$$g_{ds} = real(Y_{22} + Y_{12}) \tag{3.4b}$$

Y-parameters measurement involves two test setups, one for each shorted port. This is also true in the simulator and while strictly speaking in terms of this research it does not cause us any more than a few repetitive calculations. However in keeping our methods generic and repeatable in the laboratory a method based on S-parameters was developed that helps streamline the measurement process. S-parameters were selected

because they are easy to measure using a Vector Network Analyzer in the laboratory and are supported by many electrical CAD simulation vendors.

Scattering parameters or S-parameters describe the electrical behavior of linear electrical networks when undergoing various steady state stimuli by electrical signals. In the S-parameter approach, an electrical network is regarded as a "black box" which interacts with other circuits through its ports [34, 35 & 36]. The network is characterized by a square matrix of complex numbers called its S-parameter matrix, which can be used to calculate its response to signals applied to the ports. S-parameters describe the response of an N-port network to electrical signals at each port. The first number in the subscript refers to the responding port, while the second number refers to the incident port. Thus S21 means the response at port 2 due to a signal at port 1.

Once the S-parameters have been measured or calculated via simulation they must be converted to Y-parameters so that we can apply equations (3.4). In ADS the conversion is facilitated by the simulator itself converting automatically during simulation the S-parameters to Y-parameters or one can use the stoy() [13] function to accomplish the same task. The equations to convert S-parameters to Y-parameters are as follows [13]:

$$D = ((1+S_{11})*(1+S_{22}) - S_{12}*S_{21}) \quad (3.5a)$$

$$Y_{11} = (((1-S_{11})*(1+S_{22}) + S_{12}*S_{21}) / D)*Y0 \quad (3.5b)$$

$$Y_{12} = (-2*S_{12} / D)*Y0 \quad (3.5c)$$

$$Y_{21} = (-2*S_{21} / D)*Y0 \quad (3.5d)$$

$$Y_{22} = (((1+S_{11})*(1-S_{22}) + S_{12}*S_{21}) / D)*Y0 \quad (3.5e)$$

In our characterization process the terminal impedances are set to Z0 = 50Ω because there needs to be a value for the port terminations in the simulator. However the characterization process can use almost any value since Y0 = 1/Z0 is used in the conversion to Y-parameters as per (3.5).

## 3.5 $I_0$ Determination using Y-parameters Method

Determination of $g_m$ using equation (3.4a) can be done using an S-parameters simulation in ADS. The S-parameters simulation setup is shown in Figure 3-14. The use of the DC_Feed components is to avoid the AC signals being grounded through the DC

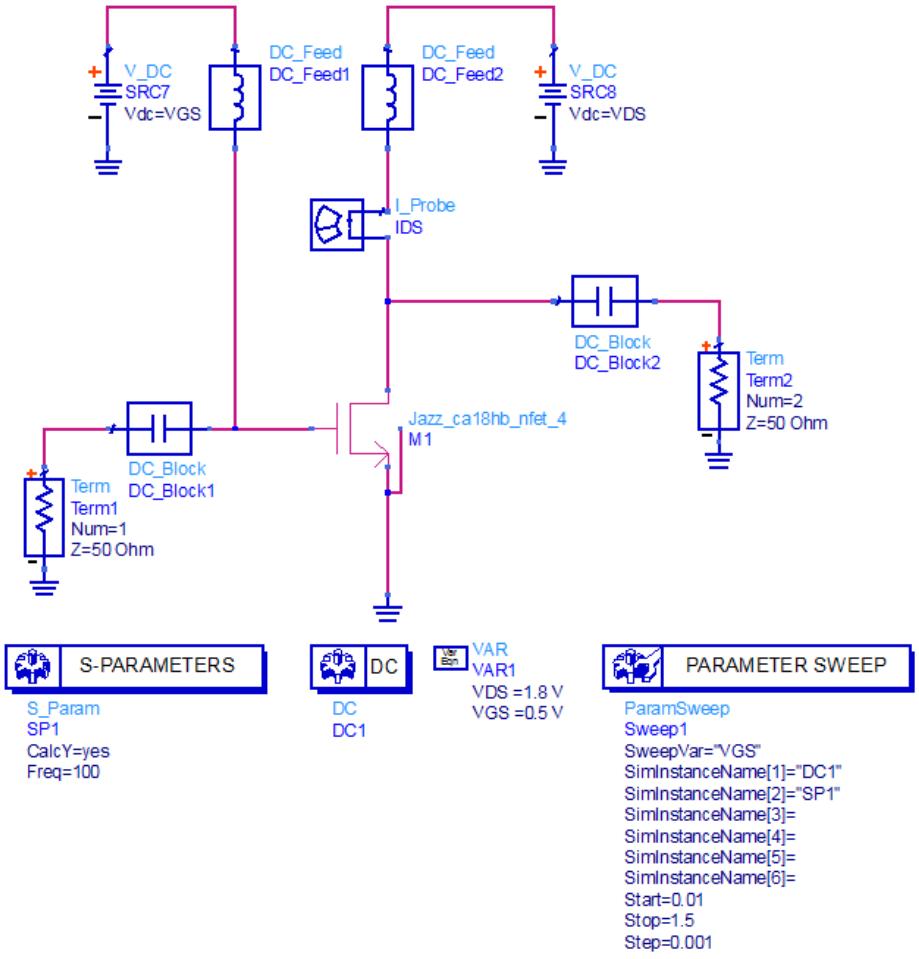



Figure 3-14 S-parameter simulation setup used for $g_m$ measurement

sources and the DC_blocks are used to block the DC bias from being shorted through the S-parameter ports [13]. In the laboratory very large inductance and capacitance values would be used to approximate these ideal components. Notice that in this setup along with the S-parameters a DC analysis is performed. This DC analysis will give us the value of the drain to source ($I_{DS}$) bias current needed to calculate the transconductance efficiency ($g_m/I_D$). The parameter sweep then performs a sweep of $V_{GS}$ for both simulations simultaneously. Notice that in effect this has taken care of the first three steps needed to determine $I_0$ as per Figure 3-1. This method has taken care of the determination of $g_m$ without having to perform a numerical differentiation which simplifies both the simulated determination of $I_0$ and the laboratory measurements and calculations as well. The results of such an analysis was post-processed in the ADS data display and the results are shown in Figure 3-15, these results are in perfect agreement as those in Figure

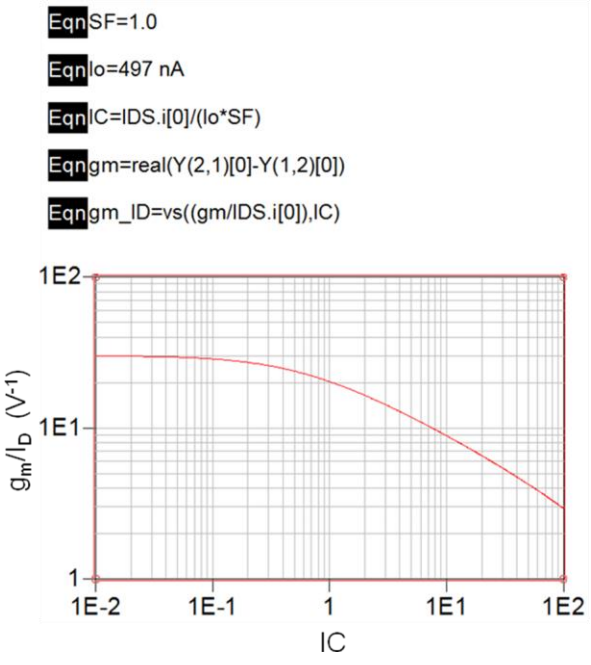



Figure 3-15 NMOS $g_m/I_D$ determination (L=4 um, $V_{DS}$=1.8V, $I_0$=497 nA) using Y-parameters

3-10. Notice that a shape factor of 1 (SF=1) and an $I_0$=497 nA value as that determined in section 3.1 were used. The remaining portion of the $I_0$ determination process as per Figure 3-1 can be performed in ADS allowing the optimizer to be the mechanism that implements the decision portion, i.e. $|\Delta Y|=0$ and subsequent $I_0$ candidate values. Optimization requires that an initial value of $I_0$ be assigned to a variable such as $I_0$ shown in Figure 3-16 and is set up to be an optimizable variable. Measurements are based on Y-parameters and the DC current. Transconductance ($g_m$) is calculated as per equation (3.4a) and the SQL is calculated as per the strong_line measurement shown in Figure 3-16. The optimization setup requires an Optimizer type, for which in this thesis, based on

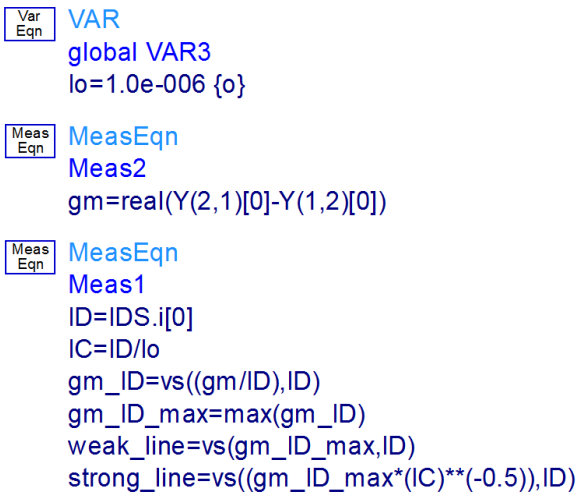
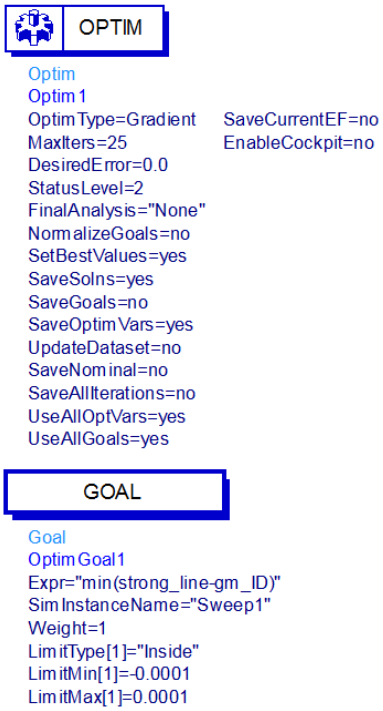



Figure 3-16 Variables and Measurements Setup for $I_0$ Determination using Optimization

our experience, the gradient optimizer performs very efficiently and is used exclusively from here on. The optimization goal implements the decision block of Figure 3-1. The reader can find the optimization setup in Figure 3-17a. The results of running this

optimization are shown in Figure 3-17b. Notice that the final error factor (FinalEF) is zero which means that indeed we have a successful optimization and $I_0$=499.2nA is the




(a)

| InitialEF | FinalEF |
|---|---|
| 9.771E-6 | 0.000 |

| optIter | OPTIM.Io |
|---|---|
| 1 | 4.992E-7 |

(b)

Figure 3-17 $I_0$ Determination via Optimization (a) ADS Optimization Simulation Setup (b) $I_0$ Optimization Simulation Results

value found. This $I_0$ value matches very well with the manual value we found as shown in Figure 3-7 and was done in a single optimization iteration which makes this method both accurate and efficient.

# 4.0 BASIC AMPLIFIER DESIGN

## 4.1 CMOS Analog Circuit Design based on $g_m/I_D$ and IC

Modern analog electronic circuits design utilizes MOSFET transconductance efficiency $g_m/I_D$ versus IC curves (as shown for instance in Fig. 3.7). Design methods based on transconductance efficiency and inversion coefficient parameters have been demonstrated in the literature [1, 3, 5, 7]. The process technology current in general is different for each semiconductor foundry and the methods shown in chapter 3 are process and model independent thus $I_0$ can be determined for any CMOS process. Once $I_0$ becomes known a circuit designer can plot $g_m/I_D$ vs. IC. Other curves, such as that of the Early Voltage (which is $g_{ds}$ normalized by $I_D$) versus IC and that of $V_{GS}$ versus IC, that are very important for analog design, can be plotted as well. Depending on the design specifications a designer using Binkley's MOSFET Operating Plane can select the channel length L and IC to intuitively optimize the sizing of each transistor in a given circuit [3, 4, 7]. The Operating Plane provides the designer with a better qualitative understanding as to how analog MOSFET performance is affected by increasing or decreasing of the inversion coefficient and the channel length.

A typical CMOS analog design has many degrees of freedom, which can often lead to much iteration and may tempt designers to use a simulator equipped with an optimizer in order to try to meet the design requirements. A consequence of such an approach is that it gives the designer little or no intuition with regards to important

tradeoffs among the four basic parameters ($I_{DS}$, L, $V_{DS}$ and IC). Our approach will allow the designer to immediately assess the tradeoff amplifier performance results based on the selected design parameters values. This is done by calculating, in real time, the amplifier gain and output resistance ($R_{OUT}$) performance measures, as well as the required design parameters $V_{GS}$ and W of each transistor.

## 4.2 Design of a NMOS Common Source Amplifier with PMOS Current Source Load

The classical gain formula for a NMOS common source amplifier with PMOS current source load shown in Figure 4-2 is [9]:

$$A_v = -g_{mn}\left(r_{dsn} \| r_{dsp}\right) \tag{4.1}$$

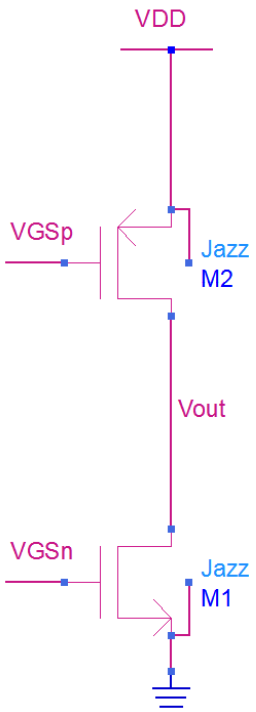



Figure 4-1 NMOS Common Source with PMOS Current Source Load Amplifier

where $g_{mn}$ is the NMOS transconductance, $r_{dsn}$ is the NMOS drain to source resistance, and $r_{dsp}$ is the PMOS drain to source resistance. The gain equation (4.1) is a result of general linear networks theorem that is independent of the transistor model being used. The theorem says that in a linear circuit the small signal voltage gain is equal to $-G_mR_{out}$, where $G_m$ is the short circuit to ground transconductance and $R_{out}$ represents the output resistance of the circuit whenever the input voltage is set to zero [9 chapter 3]. In the present work level 1 model is never used because it is considered reasonable only for technologies no smaller than 2 μm, however it is very useful for general understanding of how CMOS amplifier circuits work. As level 1 models feature a constant channel length modulation coefficient λ, (4.1) can be modified as follows:

$$A_v = -g_{mn}\left(\frac{1}{g_{dsn}+g_{dsp}}\right) = -\frac{g_{mn}}{I_D}\left(\frac{1}{\lambda_n+\lambda_p}\right) \tag{4.2}$$

Recalling that $r_{ds} = \frac{1}{\lambda I_D} = \frac{1}{g_{ds}}$ then if one wants to increase the gain it can be done by increasing the channel length L since the channel length modulation coefficient is inversely proportional to L but such design tradeoff is not obviously visible in (4.2). An alternative method of tweaking up the gain is to increase $g_{mn}$, which amounts to a reduction of $V_{GS}$. This design tradeoff can be observed on Binkley's MOSFET Operation Plane which is used extensively throughout this dissertation.

An alternate way of representing the gain is given by:

$$A_v = -\frac{g_{mn}}{g_{dsn}+g_{dsp}} = -\frac{g_{mn}}{I_D}\cdot\frac{1}{\frac{g_{dsn}}{I_D}+\frac{g_{dsp}}{I_D}} \tag{4.3}$$

where $I_D$ is the amplifier drain quiescent current. The significance of equations (4.3) stems from the MOSFET characterization $g_m/I_D$ and $g_{ds}/I_D$ graphs developed in chapter 3. Section 4.2 and the MOS Operating Plane [3] form the basis for a step by step design methodology for the design of this amplifier to be developed next.

The design methodologies presented in this research are based on the shape of the transconductance efficiency $g_m/I_D$ vs. IC graph and the current normalized output conductance curve $g_{ds}/I_D$ vs. IC. We focus our attention on submicron channel lengths. In reference [12] the authors explain that normal electrical field lines emanate from the gate towards acceptor atoms residing in the depletion region located immediately underneath the gate. These field lines correspond to the thin gate oxide capacitance ($C_{OX}$). However there are additional field lines coming out from the gate and terminating on the sides of the channel. These constitute what is called a fringing field. If W is sufficiently large then these fringing fields are a small percentage of the total electrical field and thus can be neglected. For smaller values of W the fringing fields cannot be ignored. The fringing fields help the vertical field deplete the region below the oxide layer and make it deeper, increasing the surface potential and helping start the inversion layer earlier. Therefore it takes a lower $V_{GS}$ to deplete the charge in order to start an inversion layer, which manifests itself as a lower effective threshold voltage. Capturing this effect is very important in characterizing a MOSFET model. The results of a repeated determination of $V_{TH}$ for several aspect ratios, using the techniques describe in Appendix C, was performed and the results are shown in Figure 4-2. Notice that this family of graphs shows a rapid increase of $V_{TH}$ vs. W/L for the smaller geometries. The designer must make sure to capture these effects by including sufficiently small W/L values especially

for the smaller value of L since these are the devices most affected by the vertical field effect. The experiment is then run until a constant region in which the value of $V_{TH}$ is constant is recorded. During the characterization phase of $g_m/I_D$ and $g_{ds}/I_D$ one wants to make sure that the aspect ratio used to characterize the process is in the constant region of $V_{TH}$ in order to perform the characterization with a device that does not suffer from fringing field reduction of $V_{TH}$.

In our research up to this point we have been using an aspect ratio of W/L=1 following the lead of the author in [2] for all device characterizations performed in that reference, which seems to be sufficient for CMOS technologies of L > 0.5 µm. As a contrast, all MOSFET transistor characterizations done in this dissertation are done with W/L>1 due to the aforementioned fringing field phenomenon. We choose to use a value that better represents the entire W design space. The only real significant change in the evaluation is to increase the aspect ratio in equation (2.1). In the remainder of this thesis a W/L=100 is used whenever we characterize a MOS device. That is, whenever we determine IC, $g_m/I_D$, and $g_{ds}/I_D$ from a given semiconductor foundry data. This selection means that whenever we have to select a $V_{GS}$ for a design that results in an aspect ratio that is small (approximately W/L < 20) we will have to tweak this value using a DC simulation to compensate for the lowering of $V_{TH}$ that occurs due to the fringing fields in order to finalize the design as seen in Figure 4-2. The value of W/L used needs only to be in the constant range of the graphs shown in Figure 4-2. We recommend using a value after which all L values are constant. In our research we used 100 but any value above W/L = 20 would have been appropriate.

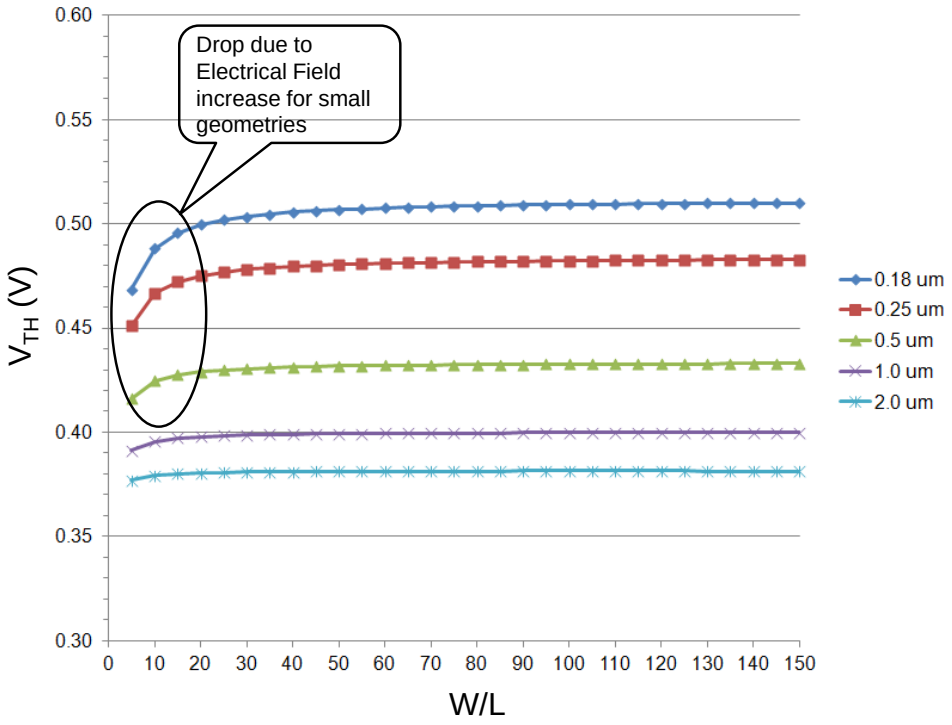



Figure 4-2 MOSFET Threshold Voltage Dependence on Aspect Ratio for TowerJazz CA18HB Process

The design variables that are used in this design methodology for each MOSFET transistor are the inversion coefficient (IC), channel length (L) and drain bias current ($I_D$). Proper selection of these design variables leads to the values for MOS channel width (W) and gate to source bias voltage ($V_{GS}$) needed to complete the design and achieve a certain desired small-signal voltage gain for the amplifier. The value of W is based on $I_D$ and IC using equation (2.1). In the characterization process the value of $V_{GS}$ has been swept and IC was thereafter calculated so that the correspondence between the values of $V_{GS}$ to IC becomes known. We next present an extension to the MOS device characterization developed so far that will add the drain to source voltage ($V_{DS}$) and the channel length (L) to the characterization.

## 4.3 MOSFET Transistor Characterization for Analog CMOS Design

The design methodology that we will use for the NMOS common source amplifier with a PMOS current source load will use the design variables IC, $V_{DS}$ and L. We hence need to know the values of $g_m/I_D$ and $g_{ds}/I_D$ across the entire variable design space. This requirement is implemented by performing these measurements for $g_m/I_D$ and $g_{ds}/I_D$ while varying these three design parameters. In a simulation we start with the setup of Figure 3-14 for both NMOS and PMOS devices. A series of nested parameter sweeps will then provide the needed characterization over the design variables space as seen in Figure 4-3. The $V_{GS}$ sweep controls the level of inversion and therefore is needed for the $g_m/I_D$ vs. IC characterization. In section 4.3 we explain that $g_{ds}$ has both $V_{DS}$ and L dependencies. It is well known [3, 7] that $g_m/I_D$ will follow a -1/2 slope as long as the

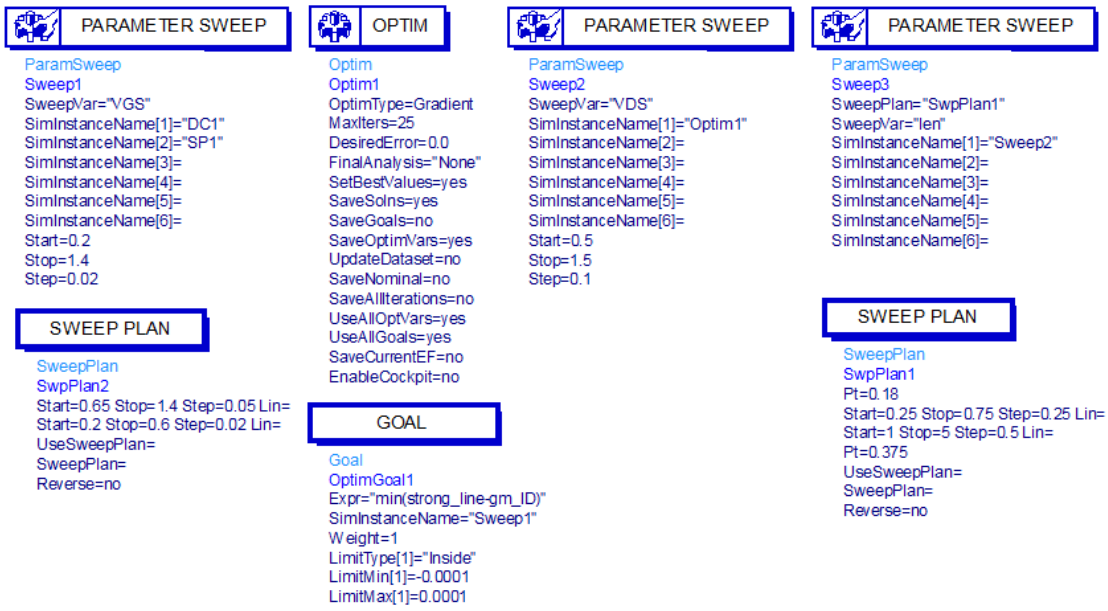



Figure 4-3 MOS Transistor Characterization Nested Sweep Setup used to determine $I_0$, $g_m/I_D$ and $g_{ds}/I_D$. The $V_{GS}$ sweep is needed to vary the level of IC. $V_{DS}$ and L dependencies are included by also sweeping these parameters.

device does not suffer from velocity saturation effects. The $g_m/I_D$ slope will increase towards -1 the smaller L and the deeper one pushes the device into the strong inversion region.

The values selected for the characterization depend on the foundry process being used. TowerJazz CA18HB 1.8V process does not allow any voltage between any of the MOS device terminals to be higher than 1.8V [14, 15]. We found after a few iterations that a range of $0.2\ V \leq V_{GS} \leq 1.4\ V$ was adequate for characterizing the MOS devices to at least cover the $0.01 \leq IC \leq 100$ range which is most adequate for analog CMOS design in our experience. Users working with other design kits should sweep $V_{GS}$ to cover the same IC range at the least. For the $V_{DS}$ sweep we wanted to make sure that the MOS device was characterized in saturation mode and that the process limits were not violated so we selected 0.5 V (triode mode boundary) $\leq V_{DS} \leq$ 1.5 V (maximum $V_{DS}$ of the transistor). The upper limit for $V_{DS}$ is selected such that enough headroom is left for the signal so that no distortion happens by driving any transistor (e.g. a load transistor) into cutoff. The lower limit for $V_{DS}$ is selected such that the transistor does not go into triode mode. A good estimate for the lower limit is to keep it above the MOS threshold voltage which, based on the TowerJazz specification, has a typical value of 0.38 V that can be used. Other foundry process electrical characterizations may yield different $V_{TH}$ values so the user should adjust the range of $V_{DS}$ sweep accordingly. We now concentrate on submicron CMOS analog design even though the TowerJazz process allows for 0.18 µm $\leq L \leq$ 150 µm. A range of 0.18 µm $\leq L \leq$ 5 µm was selected for the characterization. We selected these limits for the channel length since 0.18 µm is the process minimum and since after L = 5 um the MOS device is considered a long channel device so that anything

we find at L = 5 μm would represent anything above it fairly well. All these limits are shown in the Figure 4-3 setup and whenever dealing with any other process they should be modified to fit the particular process as we have done for the CA18HB TowerJazz process.

Notice that in Figure 4-3 the Optimization option was kept. The reader may recall that this optimization was included for the determination of $I_0$. However as we showed in Chapter 3 that $I_0$ needs to be extracted for a sufficiently large device $L \geq 2\mu m$ and for $V_{DS} \geq 0.5$ V. The reason that we still do $I_0$ determination below these limits is that we wish to study the impact on the design of our target amplifier should these limits are not obeyed.

## 4.4 NMOS CS with PMOS Current Load Amplifier Design

The design of a NMOS common source amplifier with PMOS current source load for a certain specified gain, computed using (4.5), is accomplished by selecting IC, L, $I_D$ and $V_{DS}$ values for each transistor in which the remaining design unknowns are $V_{GS}$ and W for each transistor. The design will be accomplished using the transconductance efficiency determined by using Y-parameter measurements of the amplifier (see Figures 3-15) and measured current normalized conductance (see Figure 4-1). Selection of the aforementioned design parameters for each transistor in Figure 4-2 has been set up in ADS such that by moving a series of sliders to select IC (and other design variables), as seen in the MOS Transistor Characterization Nested Sweep Setup of Figure 4-4, the designer can immediately see the impact that such a selection has on the four design parameter unknowns and the voltage gain of the amplifier, as shown in the NMOS CS with PMOS Current Load Amplifier Design Figure 4-5. Equations that post-process the

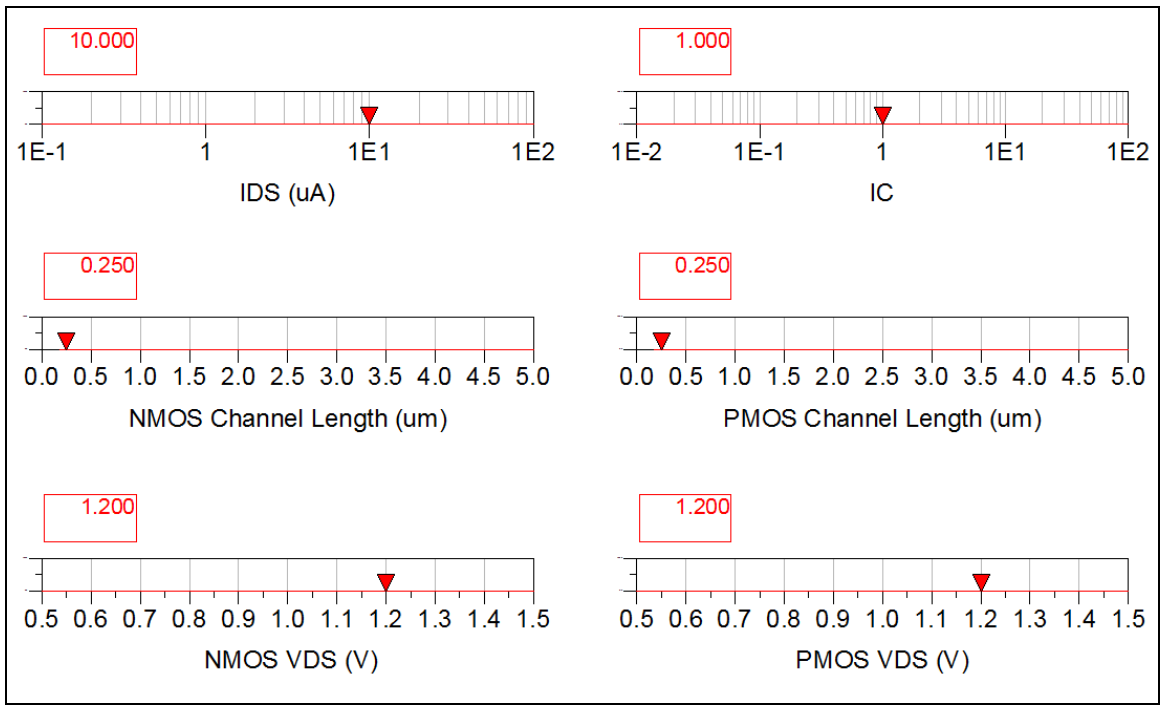



Figure 4-4 NMOS CS with PMOS Current Load Amplifier Design – Sliders Setup

results of the MOS characterization, discussed in section 4.4, are used to calculate the needed design parameters (refer to Appendix B for the details).

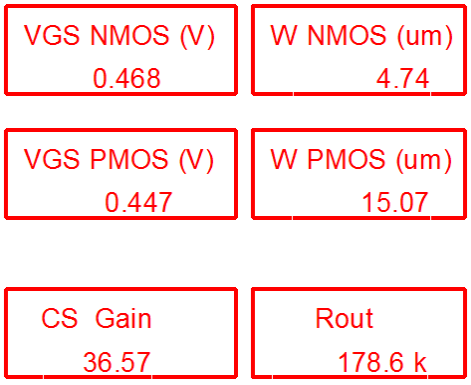



Figure 4-5 NMOS Common Source with PMOS Current Source load Amplifier Design Parameters, Gain and Output Resistance ($R_{OUT}$)

The amplifier of Figure 4-2 requires that both transistors have the same $I_D$ and therefore only one slider is needed for the current. The inversion coefficient is set the same for all the transistors of the entire amplifier as well. In a strict sense this is not a hard requirement that both transistors have the same IC. There may be cases in which the transistors may not have the same IC. For instance, in the CS amplifier the two DC gate voltages may be created using two diode-connected NMOS transistors in series. In our set up we study a configuration in which we assume that both transistors are at the same IC. Another situation is that of a CS amplifier with a diode connected load that will require different IC value for the NMOS and the PMOS. In chapter 6 we illustrate such a case when designing an OTA. The remaining parameters (i.e. L and $V_{DS}$) do not have to be the same for both transistors hence a slider for each transistor is allocated. We do note that the designer must make sure that the value of $V_{DD}$ is commensurate with the technology being used. That is, the user needs to make sure that the voltage between the MOSFET pins are not exceeded for the process being used. Clearly the design of this basic amplifier to meet a single specification, which is a required voltage gain, has many degrees of freedom which can lead to much iteration. The approach shown in Figure 4-4 allows the user to immediately see the tradeoff results of the selected values by calculating in real time, by moving the sliders, the amplifier gain, output resistance ($R_{OUT}$) and the required $V_{GS}$ and W of each transistor as seen in Figure 4-5. Refer to appendix B for explanation of ADS post-processing implementation that leads to the results shown in Figure 4-5.

The slider setup shown in Figure 4-4 results in a design that requires the $V_{GS}$ and W values shown in Figure 4-5 showing a voltage gain as predicted by the voltage gain

formula (4.4). We then put together an ADS simulation to test the design as designed. The design setup is shown in Figure 4-6. Notice that there are two identical schematics

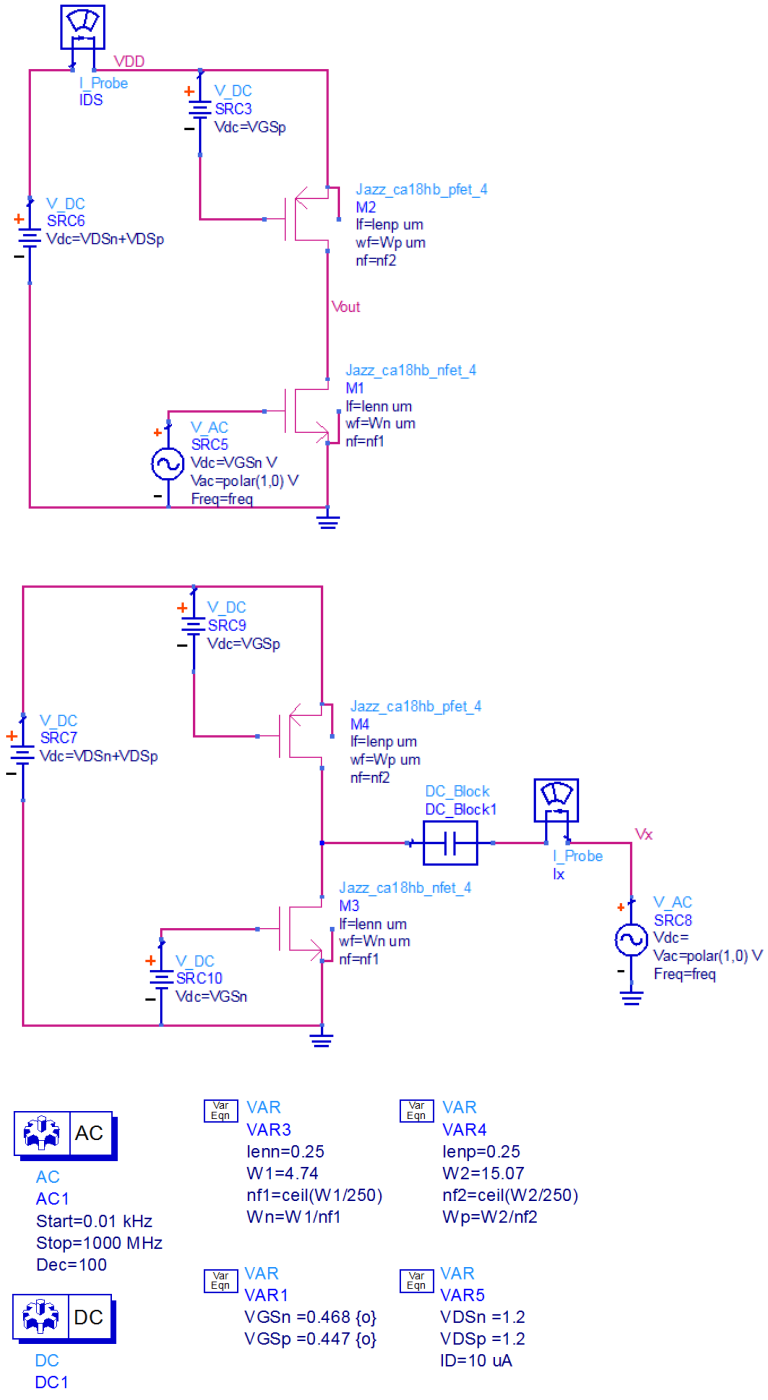



Figure 4-6 NMOS Common Source with PMOS Current Source load Amplifier Design Verification Setup

and all parameters are set up using variables to make sure that both circuits have the same parameters. The top design is used to measure the voltage gain and bandwidth of the amplifier and the bottom design is used to measure the output resistance ($R_{out}$) of the amplifier.

The results of this simulation are shown in Figure 4-7. By looking at the results we conclude that the predicted gain using the slider setup has a -3.06% (100*(35.45-36.57)/36.57) error and the predicted $R_{out}$ has a -3.96% (100*(171.5-178.6)/178.6) error. Both these errors are acceptable in most applications as both indicate that the optimal design is within easy tweaking action from the predicted design. The errors are mostly due to round off errors in the calculations primarily due to less significant digits in the various $V_{GS}$ values and also due to the fact that linearized models are used for the

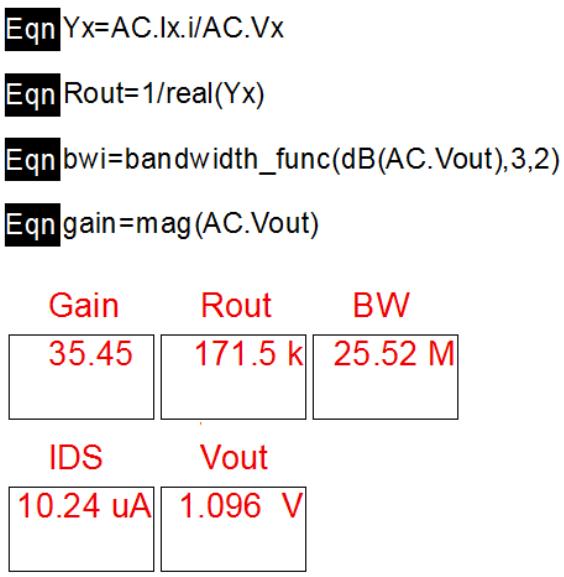



Figure 4-7 Results of Simulation for Common Source with Current Source load Amplifier

prediction and for the MOSFET characterization process . To better understand these errors we note that the $I_{DS}$ current is actually not equal to 10 µA as per the design. It is measured to be equal to 10.24 uA and the DC voltage identified on the schematic as $V_{out}$ is actually the $V_{DS}$ voltage of M1 which should be equal to 1.2 V but ends up being equal to 1.096 V. These small differences are causing most of the error in our two parametric measurements and can be corrected by some fine tweaking which we decided to do using an optimizer as the setup shown in Figure 4-8. The optimizable variables are the two $V_{GS}$ voltages for the MOS transistors and we allowed a range from 0.2 V to 1.5 V. Optimized values for $V_{GSn}$=0.4649 V and $V_{GSp}$=0.4468 V, which are very small corrections (just a few mV) to the predicted values which indicates a possible round off error. The voltage gain and $R_{out}$ errors obtained for an amplifier that is optimized to better adhere to the design predicted design parameters are -0.56% and -0.45% respectively.


Figure 4-8 Optimization Setup and Results for Common Source with Current Source load Amplifier

We should note that the bias of the NMOS Common Source with PMOS Current Load Amplifier of Figure 4-1 is not well defined. This amplifier is reliably biased only if a DC feedback is applied that forces the drain voltage to a known value. In the optimization routine that we are using the optimizer is assuming the role of the DC feedback circuitry doing fine tuning of the $V_{GS}$ voltages.

## 4.5 Incorporating Process Tolerances into the Amplifier Design Process

One advantage of using a Design Kit from the foundry (i.e. CA18HB from TowerJazz) is that the process tolerances (represented by the fast/slow corners) can be included during the design process. In this experiment both transistors are assumed to be at the same type of corner (either both are fast or both are slow), i.e. the fast-slow and slow-fast corner combinations are not considered a practical scenario. This approach is justified because in the actual process the NMOS and PMOS variation are not independent of each other [see 5 ss. 14.3]. Table 4-1 shows the estimated values for the amplifier's voltage gain, transconductance efficiency of each transistor and the current normalized drain to source conductances ($g_{ds}/I_D$) for the process corners. In this section the value of the Technology Current is recalculated for both the slow and fast corners for the NMOS and PMOS transistors. We later run a similar analysis in which we used a single value of $I_0$ taken from the nominal devices and we were able to show that a single value of $I_0$ per transistor type is sufficient to perform CMOS analog circuit design that incorporates process corners.

The estimated voltage gain was obtained by direct application of equation (4.3) and is further discussed in Appendix B. For this experiment the amplifier was designed as

per Figure 4-4. An interesting fact is that the gain (both estimated and simulated) is higher for the slow corner and lower for the fast corner when compared to the nominal process. Notice how the slow/fast simulated current changes from that of the nominal process. The slow process has a lower current and therefore the Inversion Coefficient of both transistors is lower which explains why the gain went up (i.e. the lower IC the higher $g_m/I_D$). For the fast process the current goes up which results in a high IC and hence a lower gain.

The results of Table 4-1 show very significant changes in the drain current. This phenomenon is due to the ±3σ process corner values. To better explain this point we refer the reader to the all-region current expression (2.10) repeated here:

$$I_{D,all} = 2n\mu C_{OX} U_T^2 \left(\frac{W}{L}\right)\left[\ln\left(1+e^{\frac{V_{GS}-V_{TH}}{2nU_T}}\right)\right]^2 \tag{4.4}$$

In [6] the author explains that for a +3σ process the values of $T_{OX}$ (oxide thickness) and $V_{TH}$ (threshold voltage) are smaller than those corresponding to a nominal process. A thinner oxide and a lower threshold voltage result in a larger current as can be determined by examination of (4.4). The exact opposite is true for the -3σ process slow process. Table 4-1 also shows changes in the IC value for the NMOS and PMOS devices that no longer are equal (i.e. IC-NMOS ≠ IC-PMOS). This is also influenced by the changes in the current mentioned above and because the ±3σ process variations are not the same for the NMOS and PMOS devices.

As shown in section 3.3 the value of the technology current ($I_0$) varies with the drain to source voltage ($V_{DS}$) and channel length (L). The amplifier design was performed allowing $I_0$ to adapt as we changed $V_{DS}$, L and the process corners. However

the impact of adapting $I_0$ is not as critical as observed all the way down to 0.25 um in our studies so far.

Table 4-1 Design Summary based on Design Selection from Figure 4-4 taking into account process corners

| Process Corner | Slow | Nominal | Fast |
|---|---|---|---|
| $I_D$ uA (simulated) | 1.84 | 10 | 38.5 |
| $(g_m/I_D)_N$ | 24.69 | 20.48 | 14.84 |
| $(g_{ds}/I_D)_N$ | 0.388 | 0.369 | 0.335 |
| $(g_{ds}/I_D)_P$ | 0.120 | 0.191 | 0.218 |
| IC (NMOS/PMOS) | 0.23/0.17 | 1/1 | 3.09/3.69 |
| Voltage Gain (estimated using sliders) | 48.6 | 36.6 | 26.9 |
| Voltage Gain (simulated to test the design) | 48.4 | 36.4 | 25.8 |

In another design experiment the value of $I_0$ was kept constant that is, we used a single long channel value of $I_0$ even for the process corners for the NMOS and PMOS transistors and the design proceeded in a very similar fashion. The values used for $I_0$ were based on those measured at $V_{DS}$=1.5 V and L=5 um, $I_0$(nmos) = 502.6 nA and $I_0$(pmos) = 121.2 nA. The design setup shown in Figure 4-4 was used and the results are shown in Figure 4-9. After running an ADS optimization to correct the values of $V_{GS}$ for both transistors the final values obtained were $V_{GSn}$=0.463 V and $V_{GSp}$=0.433 V and the gain was 37.6 V/V, as seen in Table 4-2.

These results are all in very good agreement with those shown in Figure 4-9. The results from Table 4-2 for the changes in current and IC follow closely those obtained in Table 4-1 and for the same reason, i.e. these differences are due to the ±3σ process corner values. We note that the differences between these two experiments are not significant, e.g. the nominal gain differences are only 2.7%. Therefore based on the results of this

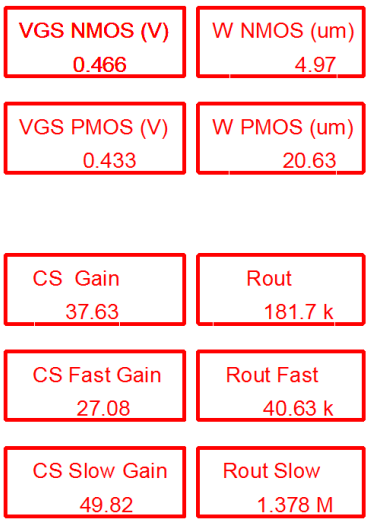



Figure 4-9 NMOS Common Source with PMOS Current Source load Amplifier Design Parameters, Gain and Output Resistance ($R_{OUT}$) with Fixed $I_0$

experiment that follow closely those of section 3.3 we conclude that using a unique long channel value $I_0$ for NMOS and PMOS devices is a proper choice, i.e. correcting $I_0$ for $V_{DS}$, channel length and process corners is not critical for analog CMOS circuit design.

Table 4-2 Design Summary based on Design Selection from Fig. 4-4 with Fixed $I_0$ and Process Corners

| | Slow | Nominal | Fast |
|---|---|---|---|
| $I_D$ uA (simulated) | 1.78 | 10 | 40.43 |
| $(g_m/I_D)_N$ | 24.81 | 20.71 | 15.02 |
| $(g_{ds}/I_D)_N$ | 0.389 | 0.370 | 0.337 |
| $(g_{ds}/I_D)_P$ | 0.109 | 0.180 | 0.218 |
| IC (NMOS/PMOS) | 0.22/0.15 | 1/1 | 3.42/4.44 |
| Gain (estimated using sliders) | 49.8 | 37.6 | 27.1 |
| Gain (simulated to test the design) | 49.8 | 37.4 | 25.8 |

## 4.6 NMOS CS Amplifier with PMOS Current Load Design Tradeoffs

The design variables used in this CS amplifier design methodology are the inversion coefficient (IC), the channel length (L) and the drain bias current ($I_{DS}$). Proper selection of these design variables lead to the values for MOS channel width (W) and gate to source bias voltage ($V_{GS}$) needed to complete the design and achieve a certain

desired small-signal voltage gain for the amplifier. The value of W is based on both $I_{DS}$ and IC using equation (2.1). In the MOSFET characterization process the value of $V_{GS}$ has been swept and the values of IC were calculated so that the correspondence between the values of $V_{GS}$ to IC became known (see Appendix B to see how it is done). The design of the CS amplifier of Figure 4-2 for a specific set gain specification can be done using the methodology of section 4.5. We now perform an experiment that will show the design tradeoffs versus IC and L for this amplifier and how the MOS Operating Plane [3, 7] is used for Analog CMOS design.

The design requirements need to tell the designer what are the maximum bias voltages available (e.g. $V_{DD}$=2.4 V). This is the starting point for the CS amplifier design of Figure 4-2. Designers must decide from the value of the available $V_{DD}$ how much DC voltage (that is, $V_{DS}$) is allocated to M1 and M2. The device characterization presented in section 4.4 is done over a set of $V_{DS}$ voltages for each device. Characterization must be done such that the maximum voltages between all pins on the device under test do not exceed foundry restrictions [14, 15]. Therefore whenever using $g_m/I_D$ or $g_{ds}/I_D$ values these choices are for a specific set of values for L, IC and $V_{DS}$. In the experiment that follows the values shown in Table 4-3 were used to for the devices.

Table 4-3 NMOS CS Amplifier with PMOS Current Load Parameters used for the design tradeoffs Experiment

| | |
|---|---|
| L (um) | 0.18, 0.25, 0.5 |
| IC | 0.01 to 0.1 in 0.01 steps<br>0.10 to 1.0 in 0.10 steps<br>1.0 to 5.0 in 1.0 steps<br>5.0 to 100 in 5.0 steps |
| $V_{DS}$ (V) | 0.5 to 1.5 in 0.1V steps |

The L and IC values need to be carefully selected based on the MOS Operating Plane. For example using TowerJazz Semiconductor foundry design kit for ADS one can design a CS amplifier with both transistors in Figure 4-2 having $V_{DS}$=1.2 V for L=0.18 µm up to L=0.5 µm and one could select a different IC for each length to get the same gain for each case. Using those techniques developed in section 4.5 an experiment is performed to validate the selection of the different design variables. The aim is to show that proper selection of these variables with the guidance of the MOS Operating Plane can be done in an almost a straightforward way. First the DC voltage supply ($V_{DD}$) is set at 2.4 V. Furthermore 1.2V is allocated for the $V_{DS}$ of each transistor of Figure 4-2 to allow a large enough swing. Bias current is set to 50µA. This current level is selected because, as the reader will see in Table 4-5, the width for the MOSFET transistors becomes reasonable. That is, need to watch that transistor dimensions do not extend to the millimeter range on one side or to W < L on the smaller side, which is not supported by the process. In a real world design the user could determine the current based on other considerations such as power consumption. In our case, because we wish to study the tradeoff when experimenting with different IC values as we do next, this was a proper current choice. In this experiment three cases are studied as per Table 4-4. The Inversion Coefficients will be set at 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, and 10, which is a very good sample

Table 4-4 CS Amplifier Test Cases

| Test Case | $L_{NMOS}$ (µm) | $L_{PMOS}$ (µm) |
|---|---|---|
| #1 | 0.18 | 0.18 |
| #2 | 0.25 | 0.25 |
| #3 | 0.5 | 0.5 |

Table 4-5 CS Amplifier Design and Simulation Results

$L_n$ = 0.18 µm
$L_p$ = 0.18 µm
$I_D$ = 50 µA
$V_{DD}$ = 2.4 V

Case #1

| IC | Wn (µm) | Wp (µm) | VGSn (mV) | VGSp (mV) | Gain (V/V) | Rout (KΩ) | BW (MHz) |
|---|---|---|---|---|---|---|---|
| 0.1 | 179.07 | 742.57 | 362 | 344 | 23.80 | 18.00 | 13.13 |
| 0.2 | 89.53 | 371.29 | 388 | 369 | 22.90 | 17.95 | 25.70 |
| 0.5 | 35.81 | 148.51 | 426 | 404 | 21.10 | 18.10 | 61.40 |
| 1 | 17.91 | 74.26 | 458 | 430 | 19.30 | 18.70 | 104.80 |
| 2 | 8.95 | 37.13 | 495 | 461 | 17.10 | 20.00 | 150.70 |
| 5 | 3.58 | 14.85 | 558 | 511 | 14.30 | 23.10 | 192.30 |
| 10 | 1.79 | 7.43 | 622 | 565 | 12.30 | 27.00 | 195.50 |

$L_n$ = 0.25 µm
$L_p$ = 0.25 µm
$I_D$ = 50 µA
$V_{DD}$ = 2.4 V

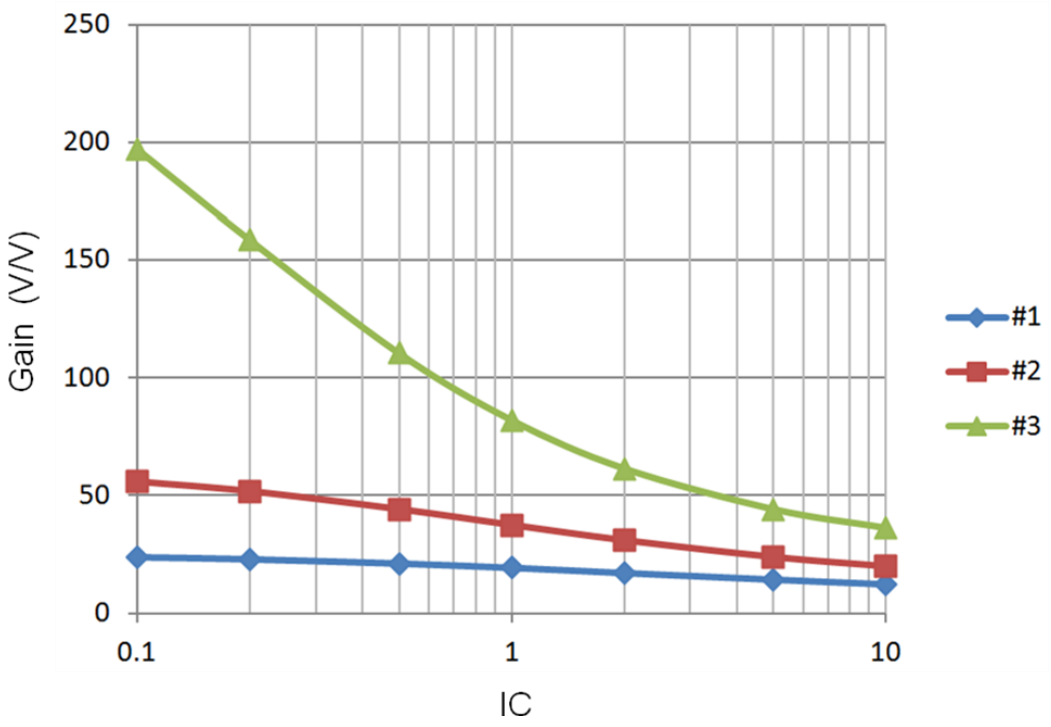
Case #2

| IC | Wn (µm) | Wp (µm) | VGSn (mV) | VGSp (mV) | Gain (V/V) | Rout (KΩ) | BW (MHz) |
|---|---|---|---|---|---|---|---|
| 0.1 | 248.71 | 1031.35 | 372 | 345 | 55.80 | 41.32 | 4.09 |
| 0.2 | 124.35 | 515.68 | 399 | 370 | 51.70 | 39.62 | 8.36 |
| 0.5 | 49.74 | 206.27 | 435 | 405 | 44.10 | 37.31 | 22.19 |
| 1 | 24.87 | 103.14 | 466 | 433 | 37.40 | 36.26 | 41.92 |
| 2 | 12.44 | 51.57 | 503 | 465 | 30.9 | 36.42 | 68.33 |
| 5 | 4.97 | 20.63 | 567 | 520 | 23.80 | 39.29 | 100.60 |
| 10 | 2.49 | 10.31 | 633 | 578 | 19.80 | 44.17 | 111.30 |

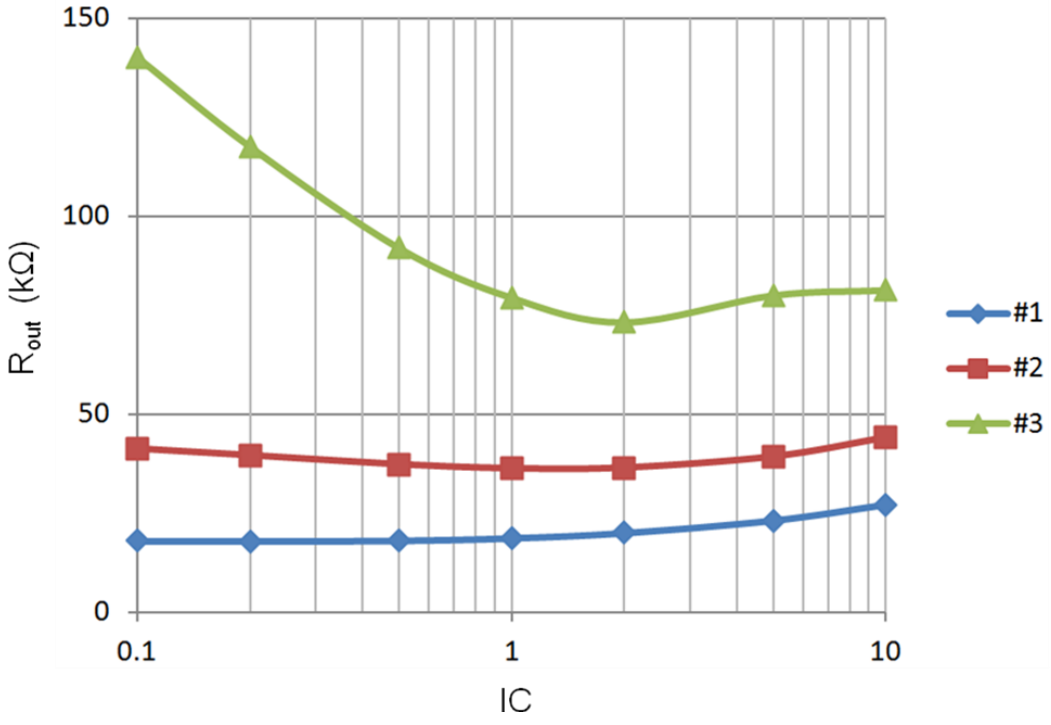
$L_n$ = 0.5 µm
$L_p$ = 0.5 µm
$I_D$ = 50 µA
$V_{DD}$ = 2.4 V

Case #3

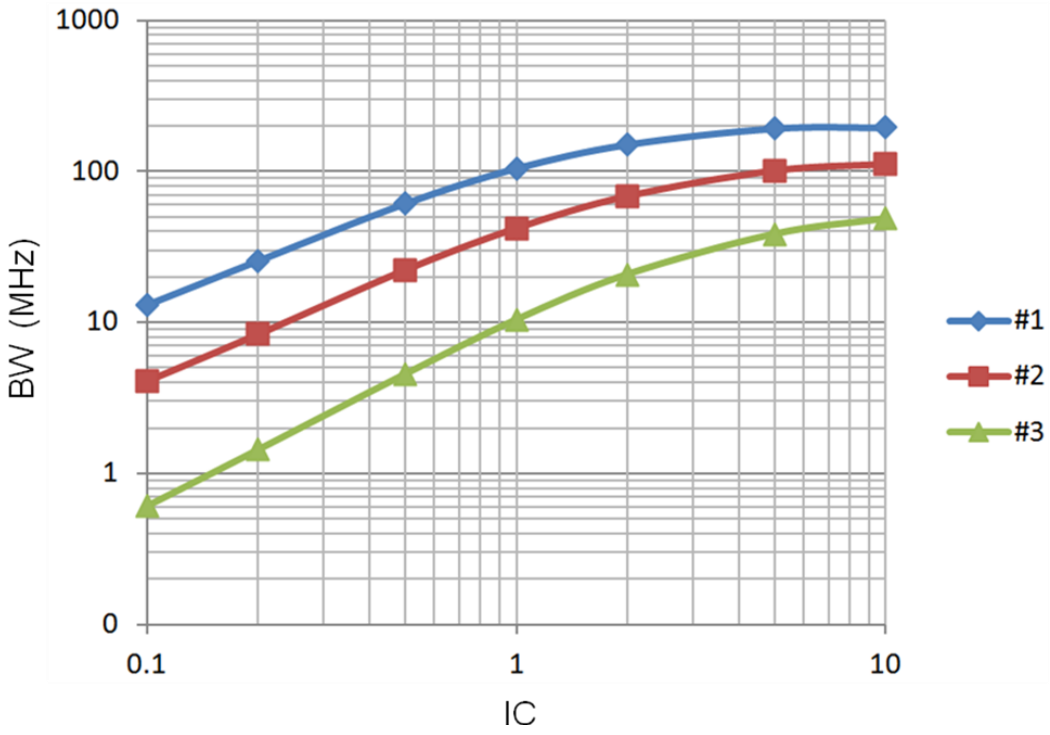
| IC | Wn (µm) | Wp (µm) | VGSn (mV) | VGSp (mV) | Gain (V/V) | Rout (KΩ) | BW (MHz) |
|---|---|---|---|---|---|---|---|
| 0.1 | 497.41 | 2062.71 | 331 | 339 | 196.90 | 140.20 | 0.61 |
| 0.2 | 248.71 | 1031.35 | 356 | 364 | 158.60 | 117.60 | 1.44 |
| 0.5 | 99.48 | 412.54 | 392 | 401 | 110.50 | 91.97 | 4.55 |
| 1 | 49.74 | 206.27 | 423 | 430 | 82.00 | 79.40 | 10.42 |
| 2 | 24.87 | 103.14 | 461 | 466 | 61.40 | 73.16 | 20.75 |
| 5 | 9.95 | 41.25 | 525 | 527 | 44.10 | 79.96 | 38.32 |
| 10 | 4.97 | 20.63 | 593 | 592 | 36.10 | 81.31 | 48.50 |


250
200
150
100
50
0
Gain (V/V)
0.1
1
10
IC
#1
#2
#3

(a)


150
100
50
0
Rout (KΩ)
0.1
1
10
IC
#1
#2
#3

(b)




(c)

Figure 4-10 CS Amplifier Experiment Results (a) Gain (b) Output Resistance (c) Bandwidth

ranging from weak inversion to strong inversion, also considering the appropriate range for low power applications [7]. Employing the sliders technique showcased in section 4-5 the width values (W) and gate to source voltage ($V_{GS}$) values for all cases were determined and are shown in Table 4-5.

In the experiment the W and $V_{GS}$ values from Table 4-5 for all the test cases are then used to build the schematic of Figure 4-5 in ADS. The designs are thereafter analyzed to determine the small signal voltage gain, the value of the output resistance and the 3 dB bandwidth. Results for all test cases are shown in Table 4-5 and are presented graphically in Figure 4-10. These results follow the tradeoffs predicted by the MOS Operating Plane. The voltage gain is higher at the lower Inversion Coefficient (IC) levels

with bandwidth (BW) having the reverse trend. Test cases 1, 2 and 3 differ mainly by the size of the channel length used which is the same for the two MOS devices as shown in each test.

Here is a summary of the main experiment results:

- Voltage gain decreases with IC and increases with channel length (L)
- Output resistance ($R_{out}$) results do not show any direct correlation with IC but $R_{out}$ does clearly increase with channel length.
- BW increases with IC and decreases with L.

These results follow exactly the trends predicted by Binkley's MOS Operating Plane. We therefore confidently say that the MOS Operating Plane and the slider setup of Figure 4-4 can be used to design a NMOS Common Source with PMOS Current Load Amplifier.

## 4.7 Cascode Amplifier Design

A Cascode amplifier with PMOS current source load is shown in Figure 4-11. By the linear circuit theorem discussed in section 4.3 and applied to the small signal equivalent circuit obtained in [33, 7 chap 3.] using the EKV model it can be proven that the gain of this amplifier is [9, 10]:

$$A_v = -g_{mn1}\left(r_{out,cascode} \| r_{dsp}\right)$$
$$r_{out,cascode} \approx \left(g_{mn2} + g_{mbn2}\right) \times r_{dsn1} \times r_{dsn2} \qquad (4.5)$$

where $g_{mbn2}$ is the body-effect transconductance of M2. This term is needed because M2 suffers from the bulk effect. In the EKV model [33] and other models like BSIM3 and PSP, the bulk effect is modeled as a dependent current source placed between the drain and the source nodes of the transistor.

As we showed for the CS amplifier with PMOS current source load the cascode amplifier gain can be determined as follows:

$$A_v = -\frac{g_{mn1}}{g_{out,cascode} + g_{dsp}} = -\frac{g_{mn1}}{I_D} \cdot \frac{1}{\frac{g_{out,cascode}}{I_D} + \frac{g_{dsp}}{I_D}}$$

*where*

$$g_{out,cascode} = \left(r_{out,cascode}\right)^{-1} \tag{4.6}$$

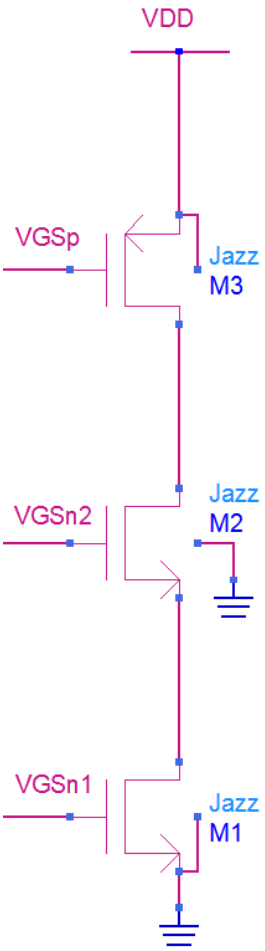



Figure 4-11 Cascode Amplifier with PMOS Current Source Load

Using equation (4.6) the cascode amplifier is designed as done in section 4.4 for the CS amplifier.

The S-parameter simulation setup, created for $g_m$ measurement shown in Figure 3-14 and equations (3.3) and (3.4), covers the case in which the MOS transistor is referenced to the source and there is no bulk effect. Examination of the circuit of Figure 4-11 (Cascode Amplifier) indicates that a bulk referenced characterization must be added because M2 suffers from bulk effect. First let us examine the small signal equivalent circuit for a MOSFET transistor with bulk effect. The equivalent small signal circuit [33] is shown in Figure 4-12.

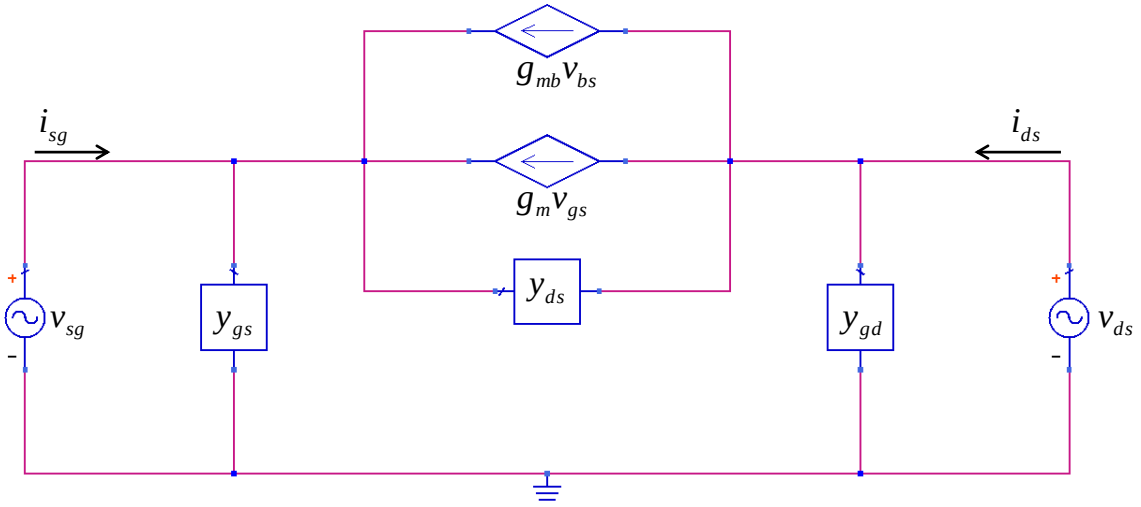



Figure 4-12 MOSFET with Bulk Effect Small Signal Equivalent Circuit

Solution of the circuit of Figure 4-12 leads to the following Y-parameter results:

$$y_{11} = y_{gs} + y_{ds} + (g_m + g_{mb}) \tag{4.7a}$$

$$y_{21} = -y_{ds} - (g_m + g_{mb}) \tag{4.7b}$$

$$y_{12} = -y_{ds} \tag{4.7c}$$

$$y_{22} = y_{gd} + y_{ds} \tag{4.7d}$$

By (4.9) the values for $g_{m,cg}$ and $g_{ds}$ are:

$$g_{m,cg} = -real(y_{21} - y_{12}) \tag{4.8a}$$

$$g_{ds} = -real(y_{12}) \tag{4.8b}$$

In the characterization procedure there is no need to separate the gate and bulk transconductances since their effects add up to what will be denoted as the common gate transconductance $g_{m,cg}$. The setup to measure the S-parameters of the common gate NMOS transistor is shown in Figure 4-13. A very similar setup is used to analyze a common gate PMOS device.

Notice that this characterization now includes the Source to Bulk voltage (i.e. $V_{SB} \neq 0$) such that the bulk transconductance ($g_{mb}$) is included in the results. This setup is a common gate setup in which the DC source to bulk ($V_{SB}$) voltage is being swept in addition to $V_{GS}$ and $V_{DS}$. We now have the capability that allows us to measure $g_m' = g_m+g_{mb}$ and $g_{ds}$ in the presence of bulk effect. The characterization technique presented in this section is used to calculate the values needed for the Cascode amplifier of Figure 4-11 and it is based on equations (4.6) as we did for the CS Amplifier that is discussed in Appendix B.

Design of the Cascode amplifier of Figure 4-11 has been set up in ADS such that by moving a series of sliders as seen in Figure 4-14 the designer can immediately see the impact that the design variable selections have on the gain of the amplifier as shown in Figure 4-15. The amplifier of Figure 4-11 requires that all transistors have the same $I_D$ therefore only one slider is needed for the current. The inversion coefficient is set for the entire amplifier as well. In a strict sense this is not a hard requirement for this amplifier.

Designers may find that under certain bias conditions M2 may require a smaller value of $V_{DS}$. In such a case, due to the bulk effect and the saturated transistor requirement, it may therefore be necessary to use different IC values for some of the transistors. For multiple

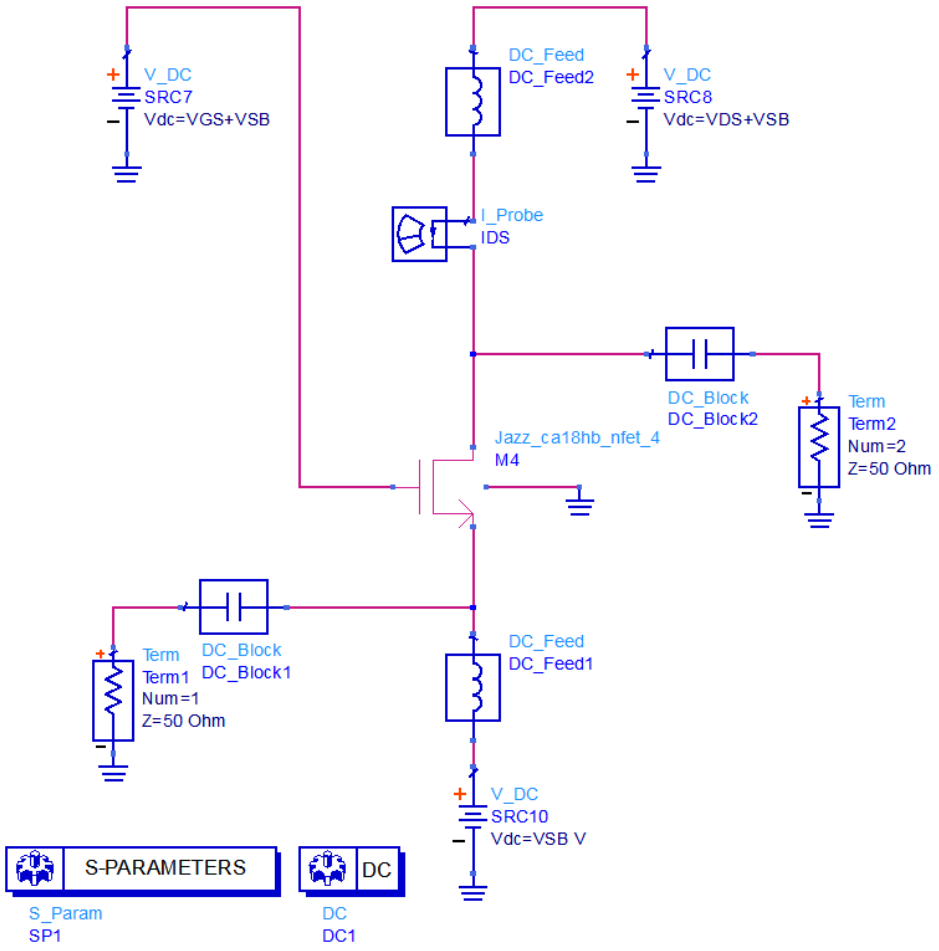
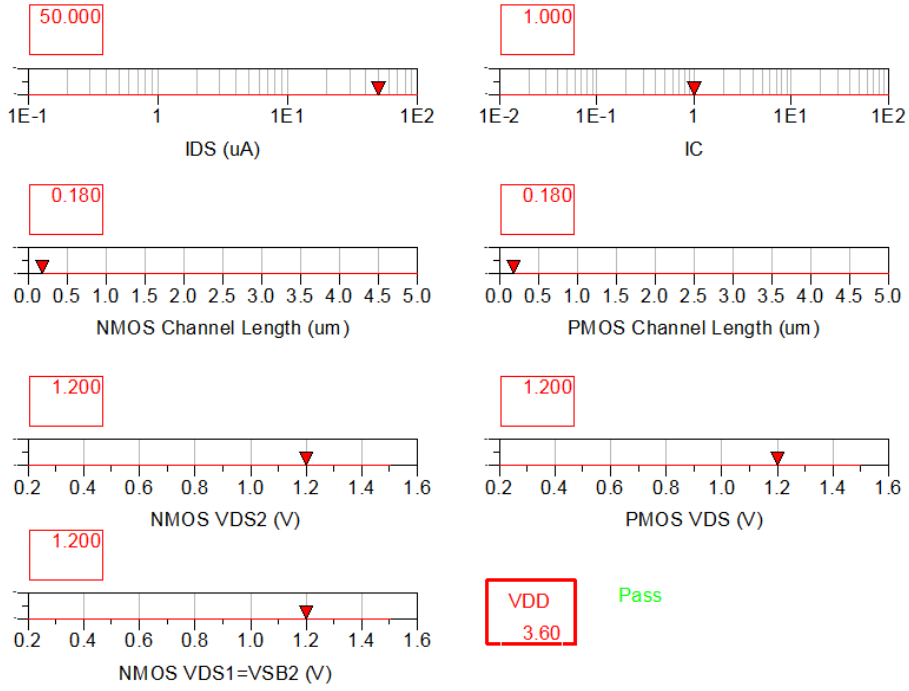
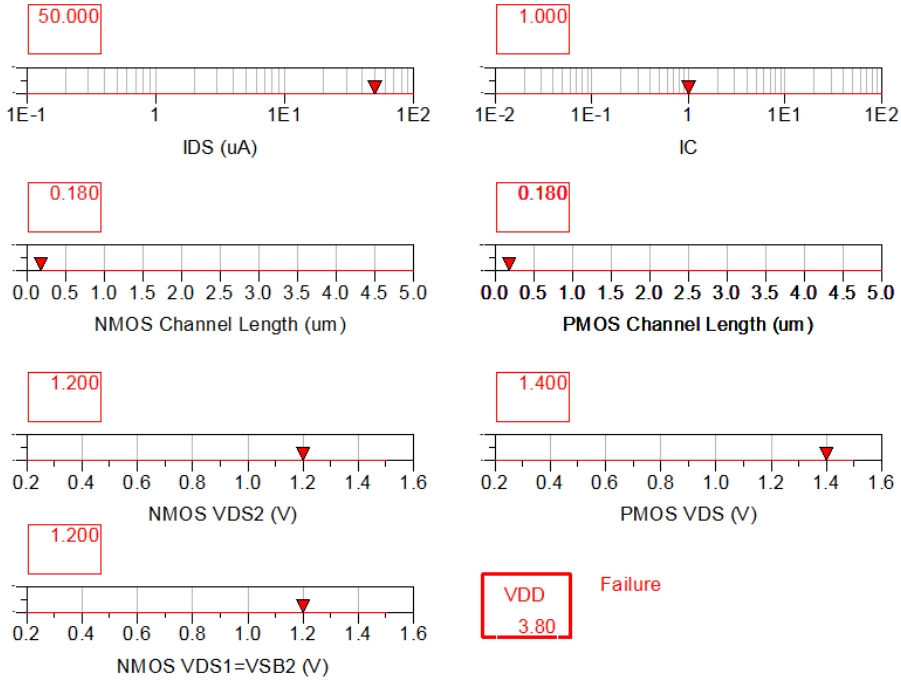



Figure 4-13 ADS MOSFET Common Gate S-parameter Setup used to Characterize Transistor with Bulk Effect

IC sliders arrangements see Chapter 6 about OTA design. The remaining parameters (i.e. L and $V_{DS}$) do not have to be the same for all transistors hence a slider for each transistor. However we did not add another slider to differentiate the L for the two NMOS transistors so both will have the same channel length. In some applications designers may find that they indeed need to increase the output resistance. Following Binkley's MOS




(a)




(b)

Figure 4-14 Cascode with PMOS Current Load Amplifier Design – Sliders setup includes a check to help the user make sure that $V_{DD}$ = 3.6V as the sliders are moved in order to meet bias requirements. The value of 3.6V is set up front by the user. (a) the sliders for $V_{DS}$ add up to 3.6V = $V_{DD}$ hence the Pass indicator (b) the sliders for $V_{DS}$ do not add up to 3.6V a Failure indicator replaces the Pass indicator.

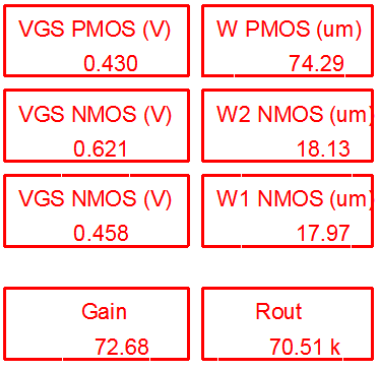



Figure 4-15 Cascode with PMOS Current Source load Amplifier Design Parameters, Gain and Output Resistance

Operating Plane the value of L of each transistor has to increase and may end up having a different L for each transistor in order to obtain an optimal design. (Reminder: M2 can be changed to increase gain via $R_{out}$ with associated impact on bandwidth). The Cascode amplifier too has a DC voltage restriction that must be accommodated by the slider design setup. Careful analysis of Figure 4-11 shows that the drain to source voltage ($V_{DS}$) of M1 is also the Source to Bulk ($V_{SB}$) voltage of M2. Therefore when selecting $g_m/I_D$ and $g_{ds}/I_D$ for M2 we set $V_{SB\_M2} = V_{DS\_M1}$. Another restriction involves $V_{DD} = V_{DS\_M1}+V_{DS\_M2}+V_{DS\_M3}$. The value of $V_{DD}$ is usually selected by overall chip bias voltages available or by power dissipation considerations. Therefore once selected the user must comply with this restriction. The slider configuration of Figure 4-14 shows the Pass/Failure indicator that helps the designer comply with the $V_{DD}$ requirement.

The slider setup shown in Figure 4-14 results in a design that requires the $V_{GS}$ and W values shown in Figure 4-15. An ADS simulation is set to test the circuit as designed. The design setup is shown in Figure 4-16. As we did with the CS amplifier design there are two identical schematics and all parameters are set up using variables to make sure

that both circuits have matching parameters. The left circuit is used to measure the gain and bandwidth of the amplifier and the circuit to the right is used to measure the output resistance ($R_{out}$).

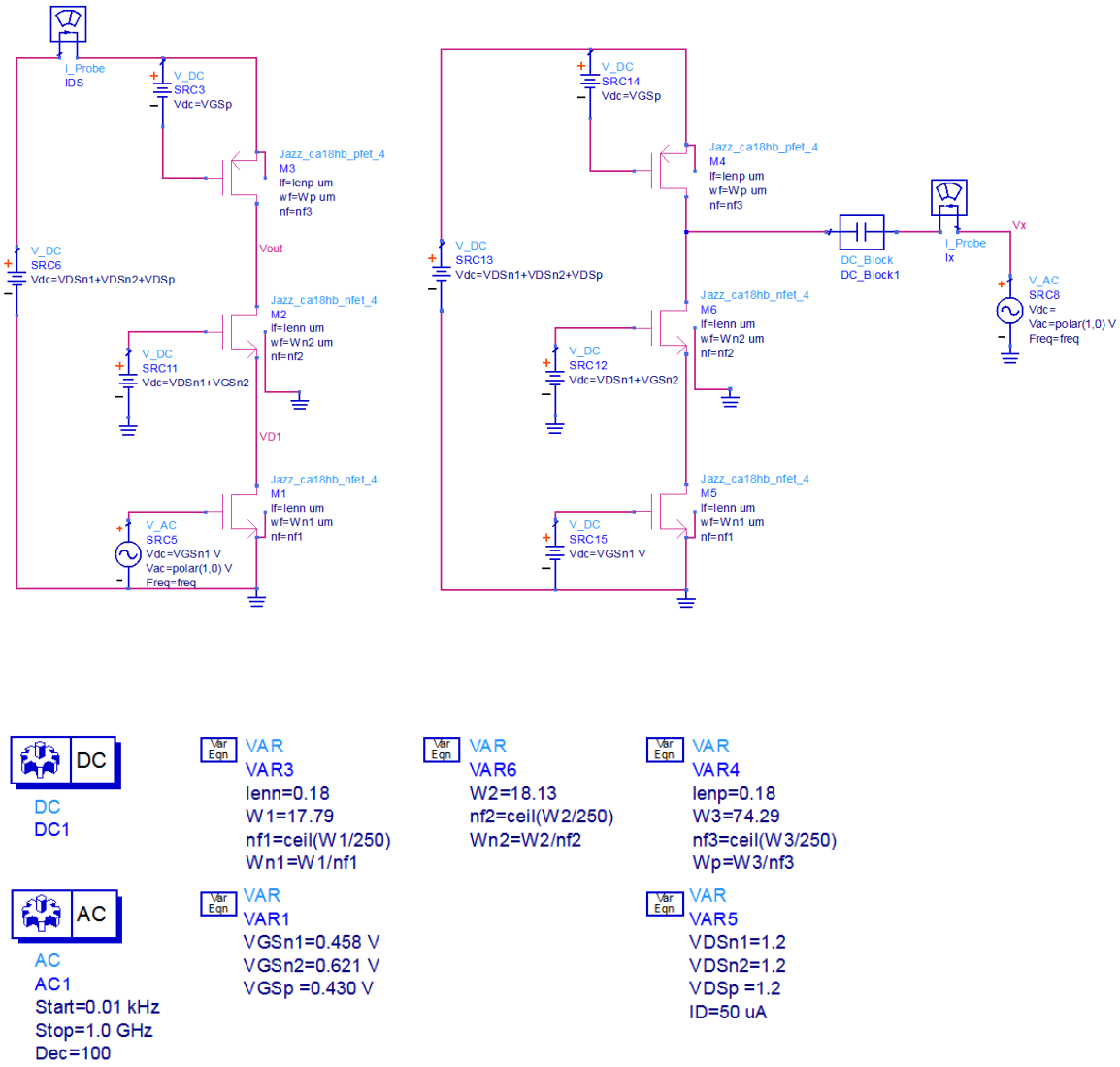



Figure 4-16 Cascode with PMOS Current Source load Amplifier Design Verification Setup

The results of this simulation are shown in Figure 4-17. We conclude by observing the results that the predicted gain using the slider setup has a 1.51% (100*(73.78-

72.68)/72.68) error compared to the actual simulated design and the predicted $R_{out}$ has a 6.8% (100*(75.30-70.51)/70.51) error. The latter error is attributed to the approximated formula taken for $R_{out}$ (4.5)).

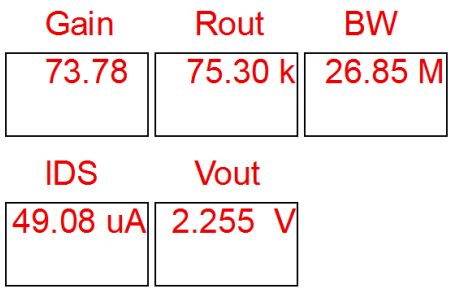



Figure 4-17 Results of Simulation for Cascode Amplifier

These errors seem similar to those obtained with the CS amplifier as noted in section 4.4. We note that the $I_{DS}$ current in Figure 4-17 is actually not 50 µA as per the design. It is measured to be 49.08 uA and the DC voltage identified on the schematic as $V_{out}$ is actually equal to $V_{DS\text{-}M1}+V_{DS\text{-}M2}$ and it should be equal to 2.4 V but it ends up being equal to 2.255 V. These small differences may be causing some of the error in our two parametric measurements and if so can be corrected by some fine tuning which in our design we decided to do using an optimizer as the setup shown in Figure 4-18. The optimizable variables are the three $V_{GS}$ voltages for the MOS transistors and we allowed a range from 0.2 V to 1.5 V. Optimized values for $V_{GSn1}$=0.4585 V, $V_{GSn2}$=0.6249 V, and $V_{GSp}$=0.4322 V, which are very small corrections (just a few mV) which indicates a possible round off error due to the large sensitivity of the design to errors in least significant digits of the $V_{GS}$ voltages. The optimized gain and $R_{out}$ did not result in any change compared to our original simulation (due to the well-known "masking" property

of cascode amplifiers). While in this case the optimizer may have not provided any measurable improvement other than to set the drain to source voltages and current to the design values it is still a very significant result that shows that in the Cascode amplifier these corrections are not as substantial as in the case of the CS amplifier.

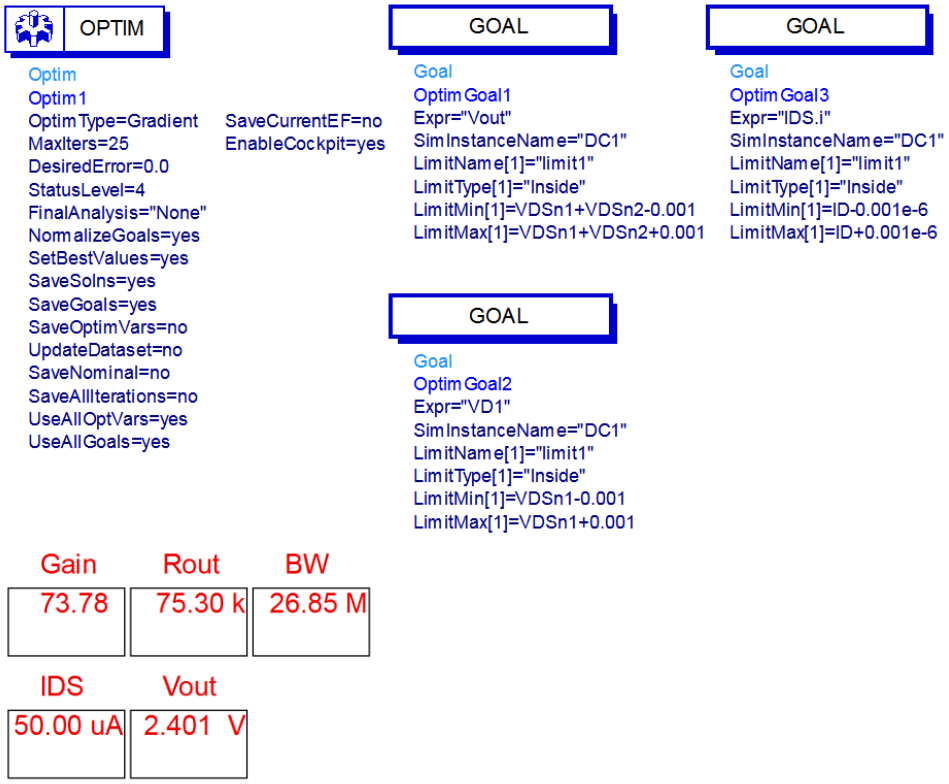



Figure 4-18 Optimization Setup and Results for Cascode Amplifier

## 4.8 CMOS Analog Design and $V_{DD}$ Impact Study

Designers often wish to push the limits of the design on many occasions due to system requirements. One such requirement is the available bias voltage on the chip. In order to study such effects we study the case in which the total bias voltage ($V_{DD}$) available to the design is 1.8V. In the Cascode with PMOS current load amplifier that we studied above the lowering of $V_{DD}$ leaves significant less voltage for the $V_{DS}$ of each of the transistors. We wish to investigate whether this may cause some of the transistors,

especially M2 Figure 4-11 to cut off causing the entire amplifier to fail catastrophically if for instance a design does not take into account the bulk effect of the cascode transistor. In order to study this effect we perform an experiment with the lower value of $V_{DD}$ of 1.8V and we sweep the IC value. In our analysis we assume a fixed load so that the PMOS $V_{DS}$ will be held at 0.8V for all tests performed. We will then assign 0.5 V equally to the two NMOS devices. In the first part of the experiment we are in search for the value of IC at which M2 first falls into triode mode (i.e. $V_{DS} < V_{GS} - V_{TH}$). Once we find the value of IC at which M2 goes into triode mode we will vary the $V_{DS}$ voltage of both NMOS transistor such that $V_{DS1} + V_{DS2} = 1.0V$.

### 4.8.1 $V_{DD}$ Experiment Part 1

The values used in this experiment are summarized in Table 6-6.

Table 4-6 Low Voltage Cascode Amplifier with PMOS Current Load Experimental Results for $V_{DD}$=1.8 V, L=0.18 µm and $I_{DS}$=50 µA

| IC | Wn1 (µm) | Wn2 (µm) | Wp (µm) | VGSn1 (mV) | VGSn2 (mV) | VGSp (mV) | Gain (V/V) | Rout (KΩ) | M1 | M2 | M3 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.01 | 1830.30 | 1904.98 | 7494.52 | 304 | 386 | 261 | 121.3 | 98.35 | Sat | Sat | Sat |
| 0.02 | 915.15 | 952.49 | 3747.26 | 326 | 410 | 286 | 118.3 | 98.46 | Sat | Sat | Sat |
| 0.05 | 366.06 | 381.00 | 1498.90 | 364 | 444 | 321 | 109.5 | 90.57 | Sat | Sat | Sat |
| 0.1 | 183.03 | 190.50 | 749.45 | 390 | 470 | 346 | 102.9 | 79.28 | Sat | Sat | Sat |
| 0.2 | 91.51 | 85.25 | 374.73 | 418 | 497 | 372 | 87.6 | 70.53 | Sat | Sat | Sat |
| 0.5 | 36.61 | 38.10 | 149.89 | 457 | 535 | 407 | 65.2 | 58.47 | Sat | Sat | Sat |
| 1 | 18.30 | 19.05 | 74.95 | 490 | 567 | 435 | 49.7 | 51.06 | Sat | Sat | Sat |
| 2 | 9.15 | 9.52 | 37.47 | 529 | 605 | 466 | 37.5 | 46.40 | Sat | Sat | Sat |
| 5 | 3.66 | 3.81 | 14.99 | 596 | 670 | 520 | 26.0 | 44.44 | Sat | Sat | Sat |
| 10 | 1.83 | 1.90 | 7.49 | 664 | 738 | 576 | 20.2 | 46.36 | Sat | Sat | Sat |
| 15 | 1.22 | 1.27 | 5.00 | 716 | 790 | 618 | 17.4 | 48.89 | Sat | Sat | Sat |
| 20 | 0.92 | 0.95 | 3.75 | 761 | 833 | 656 | 15.5 | 51.43 | Sat | Sat | Sat |
| 25 | 0.73 | 0.76 | 3.00 | 801 | 872 | 690 | 14.1 | 53.76 | Sat | Sat | Sat |
| 30 | 0.61 | 0.63 | 2.50 | 838 | 908 | 721 | 13.1 | 55.83 | Sat | Triode | Sat |
| 35 | 0.52 | 0.54 | 2.14 | 873 | 942 | 750 | 12.2 | 57.85 | Sat | Triode | Sat |
| 40 | 0.46 | 0.48 | 1.87 | 906 | 975 | 777 | 11.3 | 59.47 | Triode | Triode | Sat |

Notice that the data indicates that M2 goes into triode mode at IC=30. However our expectation of a catastrophic failure proved to be incorrect as the gain had already begun to significantly drop in the mid inversion region as seen in Figure 4-19 which follows the drop in $g_m/I_D$ of M1 as expected. In fact we notice that the gain does not suffer any further significant drop after M1 goes into triode mode at IC=40. In summary we notice a graceful drop in gain as transistors M1 and M2 go into triode mode as we increase IC.

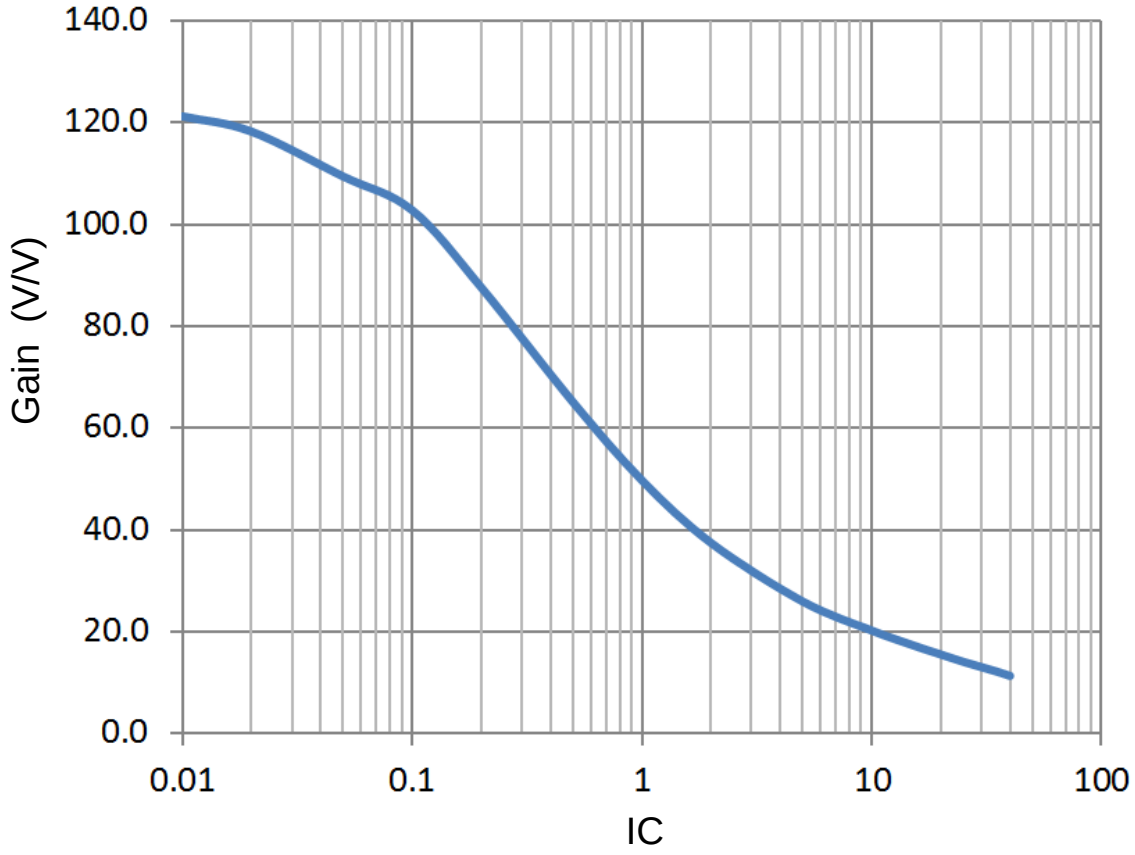



Figure 4-19 Low Voltage Cascode Amplifier with PMOS Current Load Simulated Gain Measurement

### 4.8.2 $V_{DD}$ Experiment Part 2 - Fixed IC

In this part of the experiment we take IC=30 since in the first part of the experiment we notice from Table 6-6 that this is the lowest IC at which M2 goes into triode mode. The summary of this experiment can be seen in Table 6-7. Notice that in this experiment $V_{DS1} + V_{DS2} = 1.0V$ as required. The gain did not vary nor do we see any catastrophic errors. The gain in fact is rather flat with some drop as either transistor $V_{DS}$ moves towards the lower voltage levels. These results clearly indicate that splitting the voltage equally among the two transistors is a wise choice especially if one could avoid having one or even both transistor go into triode mode. This experiment also shows that one can be very aggressive (i.e. setting the voltages close to the limits) when it comes to the bias voltage because there are no sudden failures of the amplifier.

Table 4-7 Voltage Gain and $R_{out}$ Simulated Experimental Results for Cascode with PMOS Current Load Amplifier IC=30, $V_{DD}$=1.8 V, L=0.18 µm and $I_{DS}$=50 µA

| VDSN1 (V) | VDSN2 (V) | Wn1 (µm) | Wn2 (µm) | Wp (µm) | VGSn1 (mV) | VGSn2 (mV) | VGSp (mV) | Gain (V/V) | Rout (KΩ) | M1 | M2 | M3 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.8 | 0.2 | 0.60 | 0.73 | 2.50 | 814 | 976 | 721 | 11.37 | 47.43 | Sat | Triode | Sat |
| 0.7 | 0.3 | 0.60 | 0.68 | 2.50 | 821 | 951 | 721 | 12.92 | 51.21 | Sat | Triode | Sat |
| 0.6 | 0.4 | 0.61 | 0.65 | 2.50 | 829 | 929 | 721 | 13.14 | 55.58 | Sat | Triode | Sat |
| 0.5 | 0.5 | 0.61 | 0.63 | 2.50 | 838 | 908 | 721 | 13.06 | 55.83 | Sat | Triode | Sat |
| 0.4 | 0.6 | 0.62 | 0.62 | 2.50 | 846 | 888 | 721 | 12.88 | 55.71 | Sat | Triode | Sat |
| 0.3 | 0.7 | 0.65 | 0.61 | 2.50 | 850 | 868 | 721 | 12.50 | 54.46 | Sat | Sat | Sat |
| 0.2 | 0.8 | 0.76 | 0.59 | 2.50 | 841 | 851 | 721 | 10.84 | 48.59 | Sat | Sat | Sat |

### 4.8.3 Low Voltage ($V_{DD}$) Distortion Experiment

We performed another experiment in which the objective is to study how much the lower supply voltage may affect the amplifier capability to amplify the signal with minimal distortion when transistor M2 goes into triode mode. In this experiment we will

take the last five entries from table 6-6 so that we can observe the transition of M2 from saturation mode into triode mode. At each value of IC we will increase the amplitude of the input signal until the output has a 10% distortion. We measure this distortion by performing a harmonic balance analysis in ADS and taking the largest harmonic value that is not larger than 10% of the fundamental tone amplitude at the output.

The results are shown in Table 6-8 and indicate that as the IC value increases so does the input amplitude needed to cause a 10% distortion at the output. This is a surprising result since we were expecting the output to have more distortion as transistor M2 slips into triode mode. We also wish to point out that this is actually predicted by Binkley's MOSFET Operating Plane. It indicates that as IC increases the value of the transconductance distortion is less which in our case translates to higher input signal that can be taken before the output distortion reaches 10%.

Table 4-8 Input Voltage Amplitude that Results in 10 % Output Distortion for Cascode with PMOS Current Load Amplifier for $V_{DD}$=1.8 V, L=0.18 µm and $I_{DS}$=50 µA in Strong Inversion

| IC | M1 | M2 | M3 | Amplitude (mV) |
|---|---|---|---|---|
| 20 | Sat | Sat | Sat | 62.340 |
| 25 | Sat | Sat | Sat | 63.990 |
| 30 | Sat | Triode | Sat | 71.990 |
| 35 | Sat | Triode | Sat | 76.360 |
| 40 | Triode | Triode | Sat | 86.360 |

## 4.9 Cascode Amplifier Design Tradeoffs

Similar experiments to the ones done on the CS amplifier in section 4.7 are performed for the Cascode amplifier of Figure 4-11. $V_{DD}$ is 3.6 V and since this amplifier uses three transistors we allocate 1.2 V for each transistor drain to source voltage. Bias

current is set at 50µA. In this experiment three cases are studied as per Table 4-6. The Inversion Coefficients are set at 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, and 10, which is a good sampling from weak inversion to strong inversion. Using the slider setup shown in Figure 4-14 the width values (W) and gate to source voltage ($V_{GS}$) values for all cases are determined and are shown in Table 4-9.

Table 4-9 Cascode Amplifier Test Cases

| Test Case | $L_{NMOS1}$ (µm) | $L_{NMOS2}$ (µm) | $L_{PMOS}$ (µm) |
|---|---|---|---|
| #1 | 0.18 | 0.18 | 0.18 |
| #2 | 0.25 | 0.25 | 0.25 |
| #3 | 0.5 | 0.5 | 0.5 |

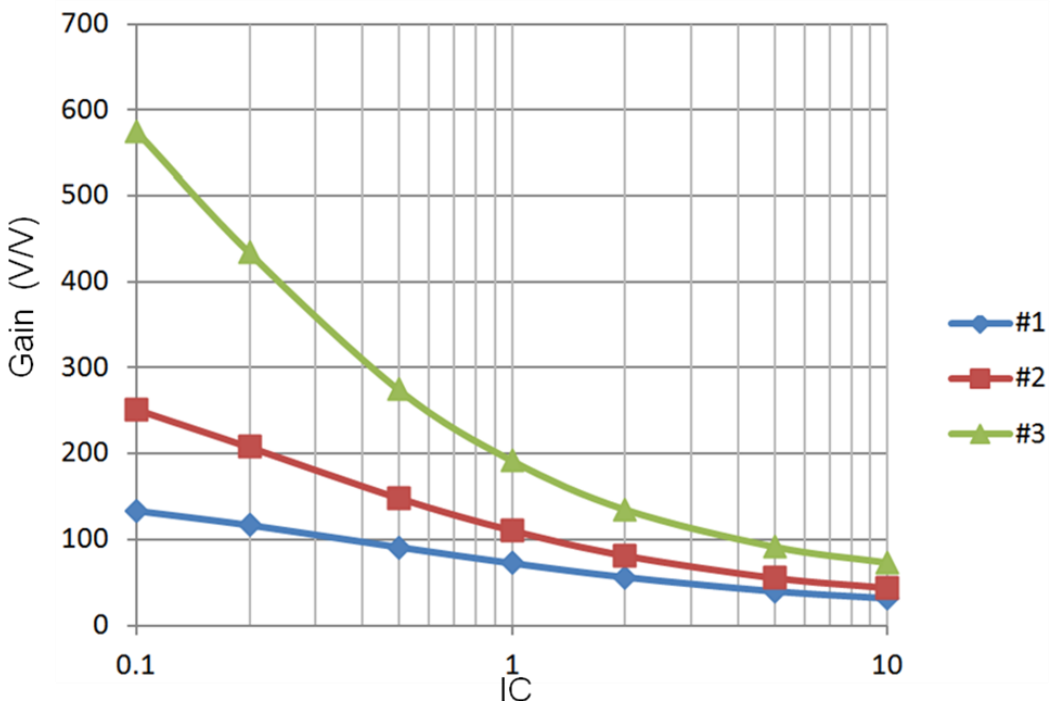
In the experiment the W and $V_{GS}$ values from Table 4-10 for all the test cases are then applied to build the schematic of Figure 4-16 in ADS. The designs are then analyzed to determine the small signal voltage gain, the value of the output resistance and the 3 dB bandwidth. Results for all tests cases are shown in Table 4-10 and and are presented graphically in Figure 4-20. These results follow the trends predicted by the MOS Operating Plane. The voltage gain is higher at the lower Inversion Coefficient (IC) levels with bandwidth (BW) having the reverse trend. Test case 1, 2 and 3 differ by the size of the channel length used which is the same for the three MOS devices as shown in each test.

The results for this cascode amplifier experiment show us that:

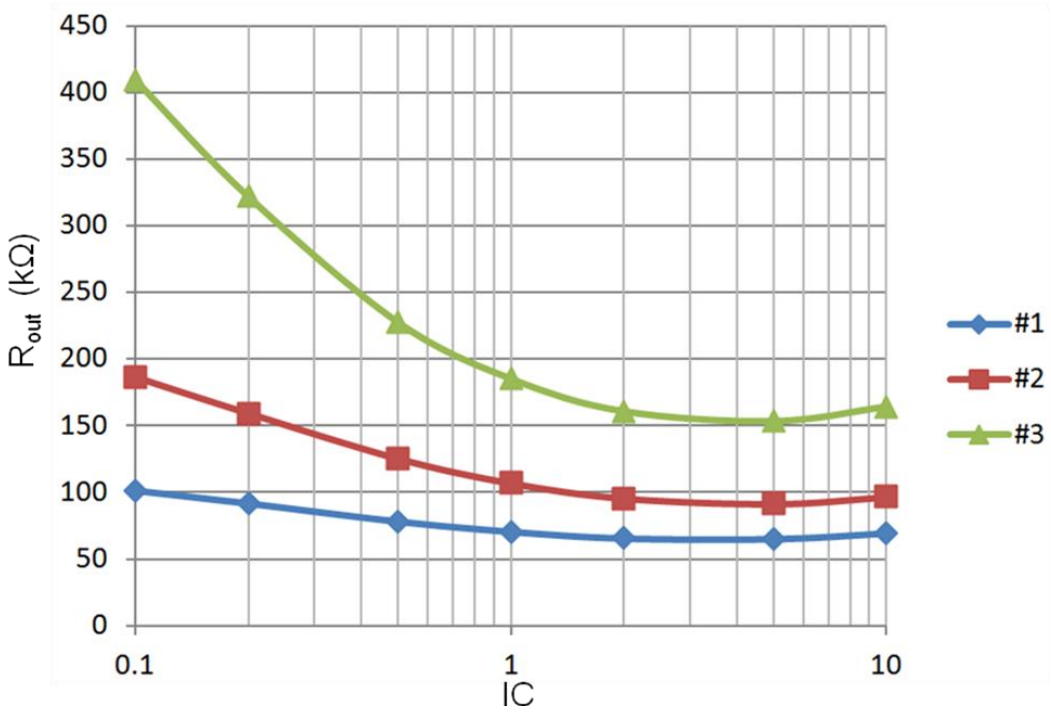
- Gain decreases with IC and increases with channel length (L)
- Output resistance ($R_{out}$) results do not show any direct correlation with IC but it does clearly increase with channel length.

Table 4-10 Cascode Amplifier Design and Simulation Results

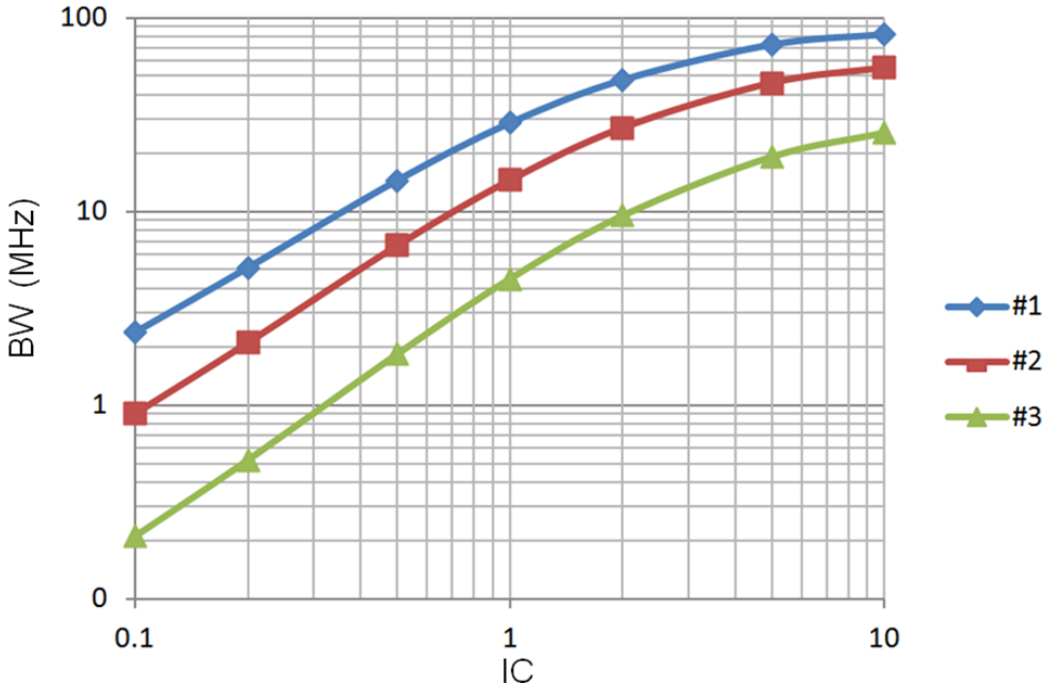
| $L_n$ = 0.18 µm<br>$L_p$ = 0.18 µm<br>$I_D$ = 50 µA<br>$V_{DD}$ = 3.6 V | | Case #1 | | | | | | |
|---|---|---|---|---|---|---|---|---|
| IC | Wn1 (µm) | Wn2 (µm) | Wp (µm) | VGSn (mV) | VGSp (mV) | Gain (V/V) | Rout (KΩ) | BW (MHz) |
| 0.1 | 179.72 | 181.28 | 742.85 | 362 | 533 | 128.80 | 100.50 | 2.37 |
| 0.2 | 89.86 | 90.64 | 371.43 | 388 | 560 | 112.60 | 90.87 | 5.12 |
| 0.5 | 35.94 | 36.26 | 148.57 | 426 | 595 | 87.83 | 77.68 | 14.44 |
| 1 | 17.97 | 18.13 | 74.26 | 458 | 621 | 69.72 | 69.92 | 28.62 |
| 2 | 8.99 | 9.06 | 37.14 | 494 | 660 | 54.20 | 65.45 | 47.85 |
| 5 | 3.59 | 3.63 | 14.86 | 558 | 722 | 38.50 | 64.86 | 72.87 |
| 10 | 1.8 | 1.81 | 7.43 | 622 | 790 | 30.20 | 69.10 | 82.40 |
| $L_n$ = 0.25 µm<br>$L_p$ = 0.25 µm<br>$I_D$ = 50 µA<br>$V_{DD}$ = 3.6 V | | Case #2 | | | | | | |
| IC | Wn1 (µm) | Wn2 (µm) | Wp (µm) | VGSn (mV) | VGSp (mV) | Gain (V/V) | Rout (KΩ) | BW (MHz) |
| 0.1 | 249.61 | 266.78 | 1031.74 | 371 | 577 | 247.30 | 185.30 | 0.91 |
| 0.2 | 124.8 | 133.39 | 515.87 | 398 | 601 | 203.60 | 158.00 | 2.11 |
| 0.5 | 49.92 | 53.36 | 206.35 | 435 | 633 | 145.10 | 124.40 | 6.67 |
| 1 | 24.96 | 26.68 | 103.17 | 466 | 664 | 108.10 | 106.20 | 14.48 |
| 2 | 12.48 | 13.34 | 51.59 | 503 | 703 | 79.60 | 95.23 | 27.00 |
| 5 | 4.99 | 5.34 | 20.63 | 567 | 764 | 54.22 | 91.27 | 46.00 |
| 10 | 2.5 | 2.67 | 10.32 | 632 | 830 | 42.30 | 96.48 | 55.16 |
| $L_n$ = 0.5 µm<br>$L_p$ = 0.5 µm<br>$I_D$ = 50 µA<br>$V_{DD}$ = 3.6 V | | Case #3 | | | | | | |
| IC | Wn1 (µm) | Wn2 (µm) | Wp (µm) | VGSn (mV) | VGSp (mV) | Gain (V/V) | Rout (KΩ) | BW (MHz) |
| 0.1 | 499.21 | 568.27 | 2063.47 | 331 | 546 | 571.40 | 407.90 | 0.21 |
| 0.2 | 249.61 | 284.14 | 1031.74 | 356 | 570 | 429.40 | 319.30 | 0.52 |
| 0.5 | 99.84 | 113.65 | 412.69 | 392 | 603 | 271.80 | 227.00 | 1.83 |
| 1 | 49.92 | 56.83 | 206.35 | 423 | 630 | 188.70 | 183.50 | 4.48 |
| 2 | 24.96 | 28.41 | 103.17 | 461 | 666 | 133.50 | 160.10 | 9.51 |
| 5 | 9.98 | 11.37 | 41.27 | 525 | 728 | 90.43 | 153.10 | 19.16 |
| 10 | 4.99 | 5.68 | 20.63 | 593 | 794 | 72.10 | 164.20 | 25.49 |


700
600
500
400
300
200
100
0
Gain (V/V)
0.1
1
10
IC
#1
#2
#3

(a)


450
400
350
300
250
200
150
100
50
0
Rout (kΩ)
0.1
1
10
IC
#1
#2
#3

(b)




(c)

Figure 4-20 Cascode Amplifier Experiment Results (a) Gain (b) Output Resistance (c) Bandwidth

- BW increases with IC and decreases with L.

These trends are very similar in nature to those of the CS amplifier and follow exactly the trends predicted by Binkley's MOS Operating Plane. We can say that the MOS Operating Plane and the slider setup of Figure 4-14 are very successful tools for the design of a Cascode with PMOS Current Load Amplifier.

A comparison between the Common Source and Cascode amplifiers studied in this chapter reveals that the Cascode amplifier has higher gain. This is mainly because in the Cascode amplifier the combination of the two transistors in cascode have a much higher output resistance than a single NMOS transistor used in the Common Source

amplifier. Therefore since both amplifiers in theory have similar transconductances the gain difference is dominated by the output resistance. The bandwidth of the Cascode is lower which in our case since the source driving the amplifiers was an ideal source (i.e. $R_{source} = 0$) favors the Common Source since the Miller Effect has no impact on the bandwidth of the amplifier. The bandwidth for common source and cascode amplifiers deserve more detailed study and involves careful consideration of the Miller Effect and to what extent it affects modern CMOS technology. We leave this topic for future research. A preliminary study included in chapter 7 was done and shows that the bandwidth improvement of a cascode amplifier over a common source amplifier depends on several parameters such as the source resistance driving the amplifier and inversion coefficient.

# 5.0 DIFFERENTIAL AMPLIFIERS

## 5.1 Differential Amplifier with PMOS Current Source Load

Differential Amplifiers are very versatile circuits used for the capacity to (in theory) provide good rejection of common mode signals coming from either radiated sources (e.g. florescent lights), power supply humming or any input signal that is common to both the inverting and non-inverting inputs. In this thesis we consider the common mode effects from input signals whenever the output of the differential amplifier is single ended (i.e. differential in and single ended out). No attempt is made to study the effect of neighboring transistor mismatch and common mode conversion, are left for future research. The basic differential amplifier studied is shown in Figure 5-1. The current source ISS shown is implemented using a single NMOS transistor current source with an ideal DC voltage source connected to the gate. Other implementations of differential amplifiers are possible using the design methodology discussed in this dissertation. For example a diode connected NMOS load would result in a different bias. Such an implementation is discussed in chapter 6 for a Simple OTA (Operational Transconductance Amplifier). Recognizing the importance of the properties of the tail current source ISS we leave more advanced current sources such as Cascode, Wilson or Widlar current mirrors as future research topics on the subject of differential amplifier design using the $g_m/I_D$ design methodology.

The classical differential gain for the differential amplifier shown in Figure 5-1 is given by [9, 10]:

$$A_{Diff} = -g_{mn}\left(r_{dsn} \| r_{dsp}\right) \tag{5.1}$$

where $g_{mn}$ is the NMOS transconductance (say for $M_1$), $r_{dsn}$ is the NMOS drain to source resistance ($M_1$) , and $r_{dsp}$ is the PMOS drain to source resistance (for $M_3$). An alternate way of representing the gain is:

$$A_{Diff} = -\frac{g_{mn}}{g_{dsn} + g_{dsp}} = -\frac{g_{mn}}{I_D} \cdot \frac{1}{\frac{g_{dsn}}{I_D} + \frac{g_{dsp}}{I_D}} \tag{5.2}$$

where $I_D$ is the amplifier drain quiescent current that flows through the M1 – M4 transistors and $I_{SS}=2I_D$. The single-ended common mode gain of the differential amplifier

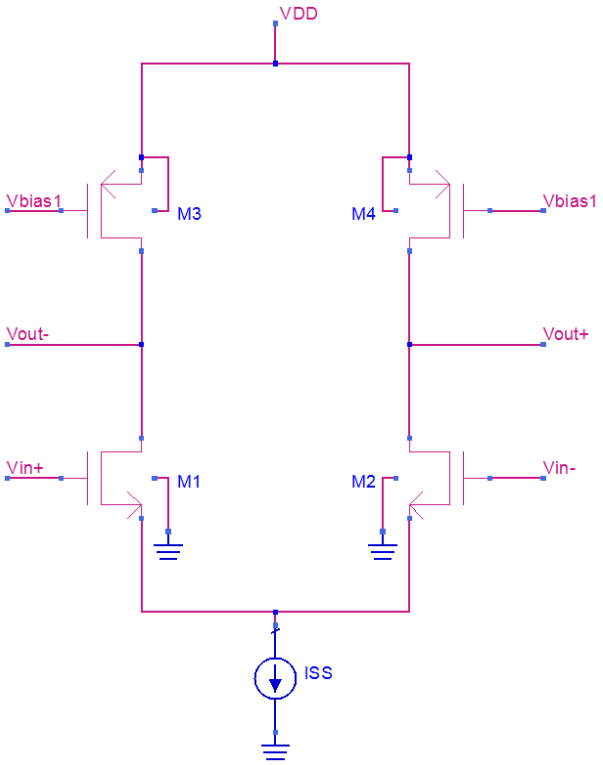



Figure 5-1 Basic CMOS Differential Amplifier with PMOS Current Load

of Figure 5-1 is given by [10]:

$$GM_{CM} = \frac{g_{mn}}{1+(g_{mn}+g_{mbn})r_{ss}+\frac{r_{ss}}{r_{dsn}}} \tag{5.3}$$

$$\frac{GM_{CM}}{I_D} = \frac{\frac{g_{mn}}{I_D}}{1+\frac{(g_{mn}+g_{mbn})}{g_{ss}}+\frac{g_{dsn}}{g_{ss}}} \tag{5.4}$$

$$Rout_{CM} = \{r_{ss}+[1+(g_{mn}+g_{mbn})r_{ss}]r_{dsn}\} \| \, r_{dsp} \tag{5.5}$$

$$\frac{gout_{CM}}{I_D} = \left\{ \frac{1}{\frac{g_{ss}}{I_D}} + \left[1+\frac{(g_{mn}+g_{mbn})}{g_{ss}}\right] \frac{1}{\frac{g_{dsn}}{I_D}} \right\}^{-1} + \frac{g_{dsp}}{I_D} \tag{5.6}$$

$$A_{CM} = GM_{CM} Rout_{CM} \tag{5.7}$$

where $GM_{CM}$ is the short circuit common mode transconductance, $Rout_{CM}$ is the common mode output resistance and $r_{ss}$ is the tail current source resistance. In most practical cases $Rout_{CM} \approx r_{dsp}$ since the term in the curly bracket in (5.5) is much greater than $r_{dsp}$. Transistors M1 and M2 suffer from the bulk effect. Recall that the bulk effect is modeled as dependent current source between the drain and the source in the EKV model [33] and other modern MOSFET models. In (5.4) and (5.6) some conductance are shown without being normalized by the drain current because the $I_D$ would cancel out. However when setting up the amplifier slider setup all these quantities are indeed normalized by the drain current.

The ratio of the desired differential gain $A_{Diff}$ to the undesired common mode gain $A_{CM}$ is an important figure of merit for differential amplifiers and is known as the Common Mode Rejection Ratio (CMRR), defined as [9, 10]:

$$CMMR = \left| \frac{A_{Diff}}{A_{CM}} \right| \tag{5.8}$$

## 5.2 Differential Amplifier Design

Design of the Differential amplifier of Figure 5-1 has been set up in ADS similar to what was done for the basic amplifiers. The differential gain is calculated using (5.2) and the single ended common mode is calculated using (5.4) and (5.6). In the corresponding formulas the transconductance efficiency and current normalized output resistance are obtained for the characterization process graphs as discussed in chapter 3.

Moving a series of sliders as seen in Figure 5-2 the designer can immediately see the impact that the design variable selections has on the amplifier differential gain, common mode gain and differential output resistance as shown in Figure 5-3. The amplifier of Figure 5-1 requires that transistors M1 – M4 have the same $I_D$ while M5 (where M5 is an NMOS current source that implements ISS) has twice the current (i.e. tail current). Therefore only one slider is needed for the current. The inversion coefficient is set for the entire amplifier as well. Again in a strict sense this is not a hard requirement for this amplifier. $V_{DS}$ is set for each pair of transistors i.e. $V_{DS\_M1}=V_{DS\_M2}$, $V_{DS\_M3}=V_{DS\_M4}$ with the same restriction applied to the channel length as shown in the slider setup of Figure 5-2. However we did add another slider to differentiate L and $V_{DS}$ of M5. This is required because M5 has twice the current and will hence require a

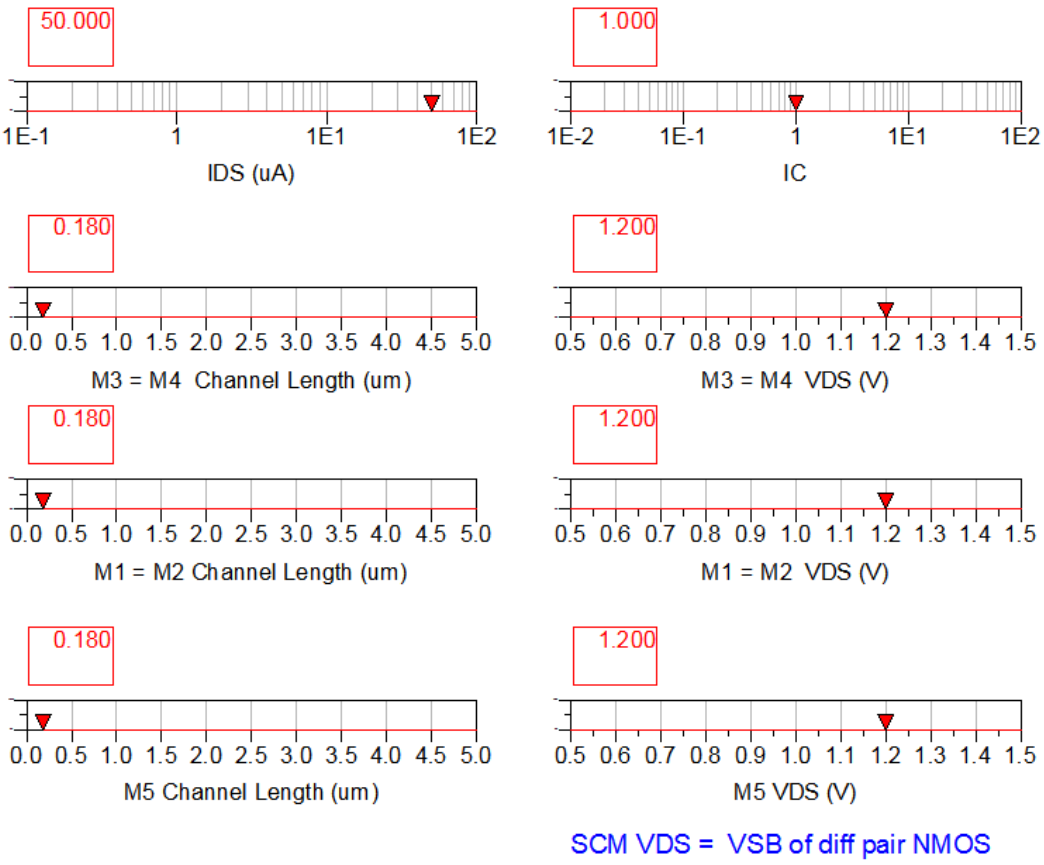



Figure 5-2 Differential Amplifier with PMOS Current Load Design – Sliders Setup

different sizing and bias than the other transistors. Also the value of this $R_{out}$ has a direct impact on the value of CMRR and we wish to control it separately. The Differential amplifier too has a DC voltage restriction that must be accommodated by the slider design setup. Analysis of Figure 5-1 shows that the drain to source voltage ($V_{DS}$) of M5 is also the Source to Bulk ($V_{SB}$) voltage of M1 (M2). Therefore when selecting $g_m/I_D$ and $g_{ds}/I_D$ for M1 we set $V_{SB\text{-}M1} = V_{DS\text{-}M5}$. This is a clear indication that for the same $V_{DD}$ the bias of the differential amplifier is more challenging and results in reduced voltage headroom for the signal being amplified when compared to the CS amplifier.

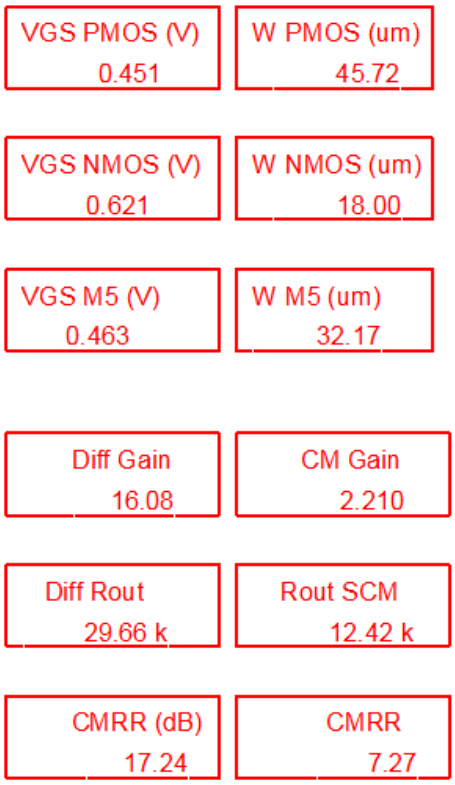
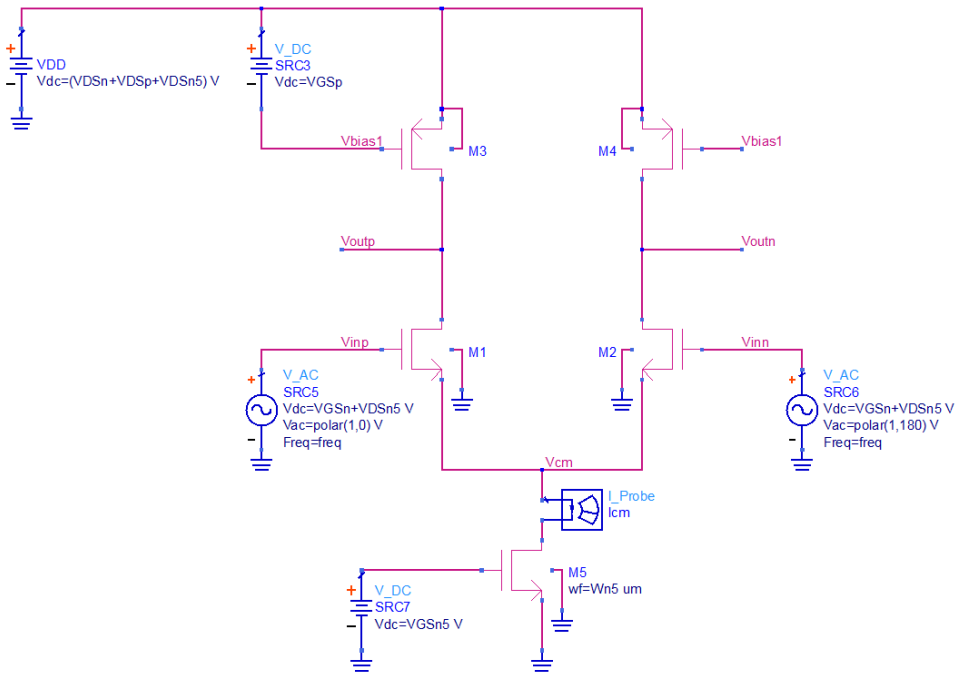
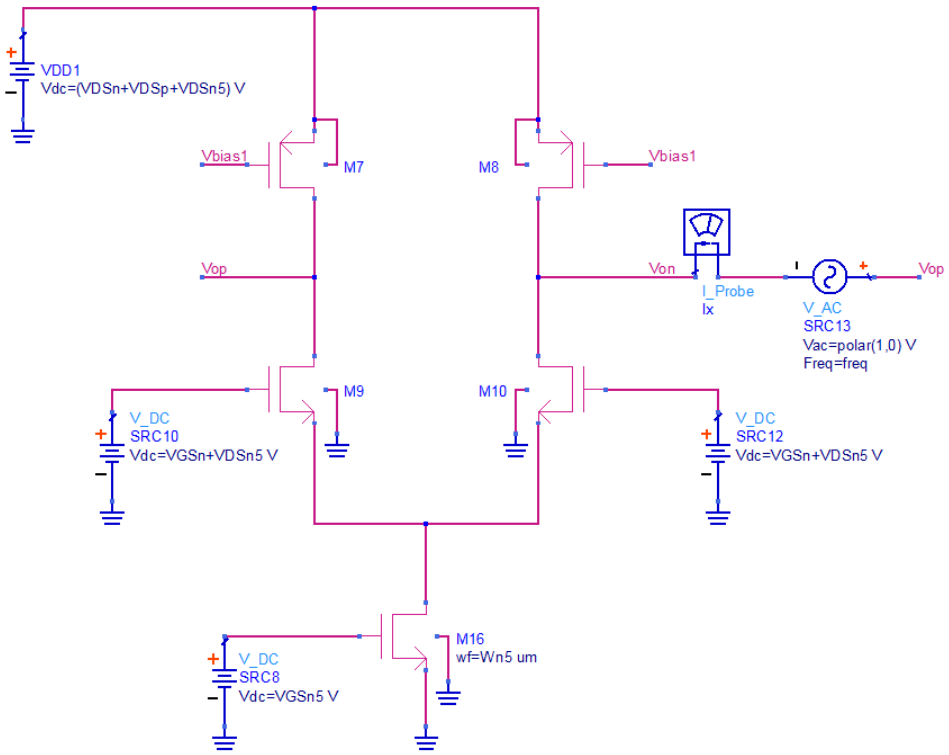



Figure 5-3 Differential Amplifier with PMOS Current Source load Design Parameters, Gain and Output Resistance

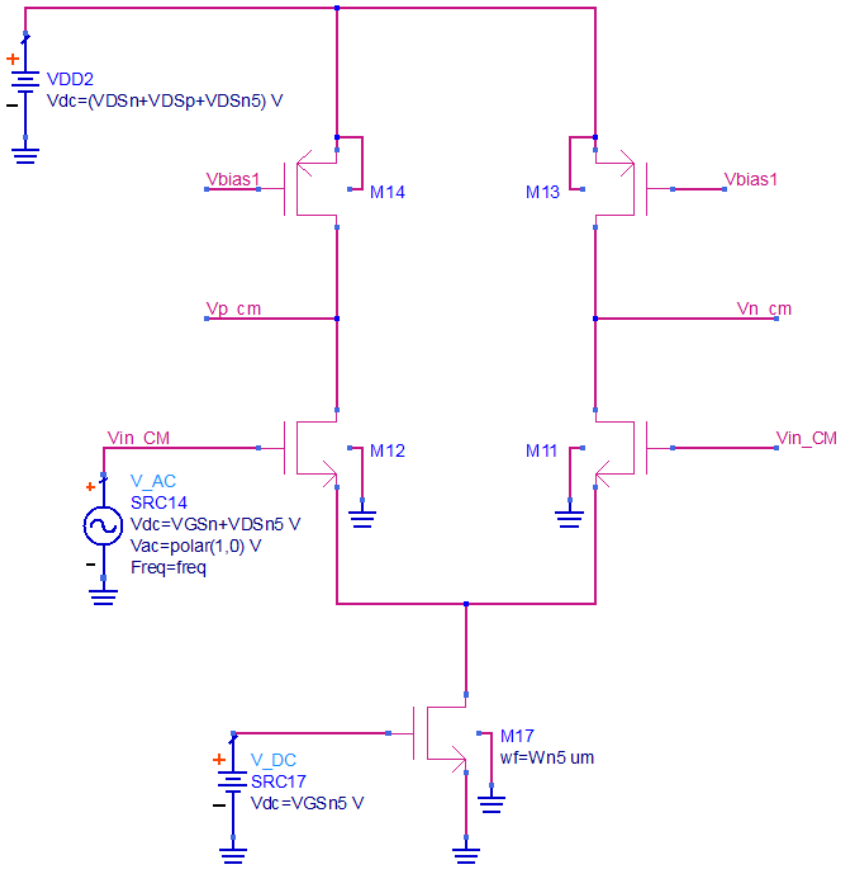
The design from the slider setup shown in Figure 5-3 is then captured in ADS to verify our design methodology. The design setup is shown in Figure 5-4. As we did with the basic amplifier designs there are several identical schematics and all parameters are set up using variables to make sure that all three circuits have the same parameters. The top design shown in Figure 5-4a is for measuring the differential gain and the differential bandwidth of the amplifier. The middle design shown in Figure 5-4b is used to measure the output resistance ($R_{out}$), and the bottom design Figure 5-4c is used to measure the common mode gain and common mode bandwidth.


VDD
Vdc=(VDSn+VDSp+VDSn5) V
V_DC
SRC3
Vdc=VGSp
Vbias1
M3
M4
Vbias1
Voutp
Voutn
Vinp
M1
M2
Vinn
V_AC
SRC5
Vdc=VGSn+VDSn5 V
Vac=polar(1,0) V
Freq=freq
V_AC
SRC6
Vdc=VGSn+VDSn5 V
Vac=polar(1,180) V
Freq=freq
Vcm
I_Probe
Icm
M5
wf=Wn5 um
V_DC
SRC7
Vdc=VGSn5 V

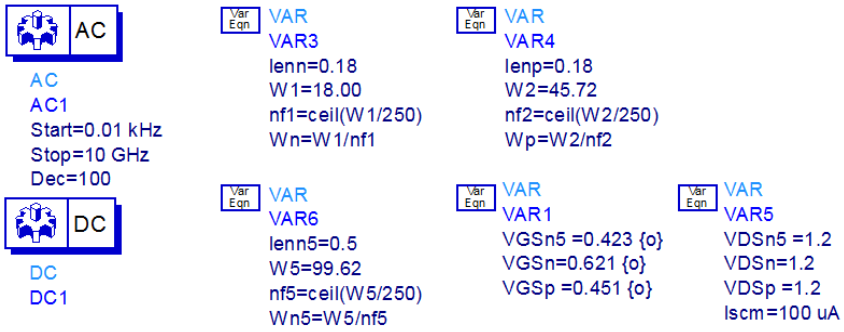
(a)


VDD1
Vdc=(VDSn+VDSp+VDSn5) V
Vbias1
M7
M8
Vbias1
Vop
Von
I_Probe
Ix
V_AC
SRC13
Vac=polar(1,0) V
Freq=freq
Vop
M9
M10
V_DC
SRC10
Vdc=VGSn+VDSn5 V
V_DC
SRC12
Vdc=VGSn+VDSn5 V
M16
wf=Wn5 um
V_DC
SRC8
Vdc=VGSn5 V

(b)




(c)




(d)

Figure 5-4 Differential Amplifier Design Verification Setup (a) Differential Gain and Bandwidth (b) $R_{out}$ (c) Common Mode Gain (d) Simulation Setup and Design Variables

The results of this simulation are shown in Figure 5-5. Notice that we expect the tail current to be 100 µA and the results show Icm=97.45 µA which we consider is acceptable and within round-off error. This small difference can be corrected by some fine tuning which we decided to do using an optimizer as the setup shown in Figure 5-6. The optimizable variables are the three $V_{GS}$ voltages for the MOS transistors and we allowed a range from 0.2 V to 1.5 V for each. The optimization resulted in very small corrections (amounting to just a few mV at the most) for each $V_{GS}$ voltage which indicates a possible round-off error. The fine-tuned $A_{Diff}$, $R_{out}$ and $A_{CM}$ did not result in

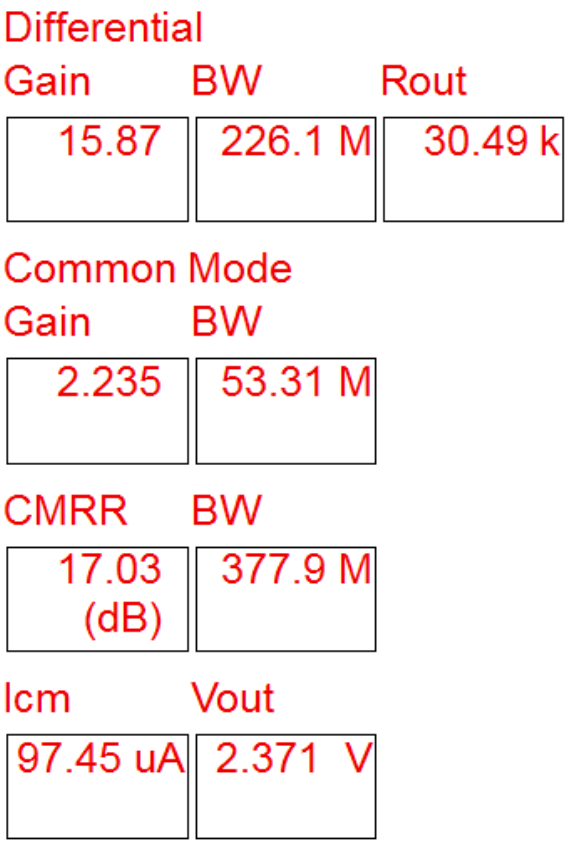



Figure 5-5 Results of Simulation for Differential Amplifier

any significant change compared to our original simulation. In this case the optimizer provided improvements to the drain to source voltages and to currents so that these match the design values. It is still a very significant observation noting that in the differential amplifier these corrections are not substantial and that the original design pre-fine tuning would perform very well. This is a result similar to the effect observed earlier involving cascode voltage shielding. Transistors M1 and M2 shield M5 from DC voltage variations at their drain node.

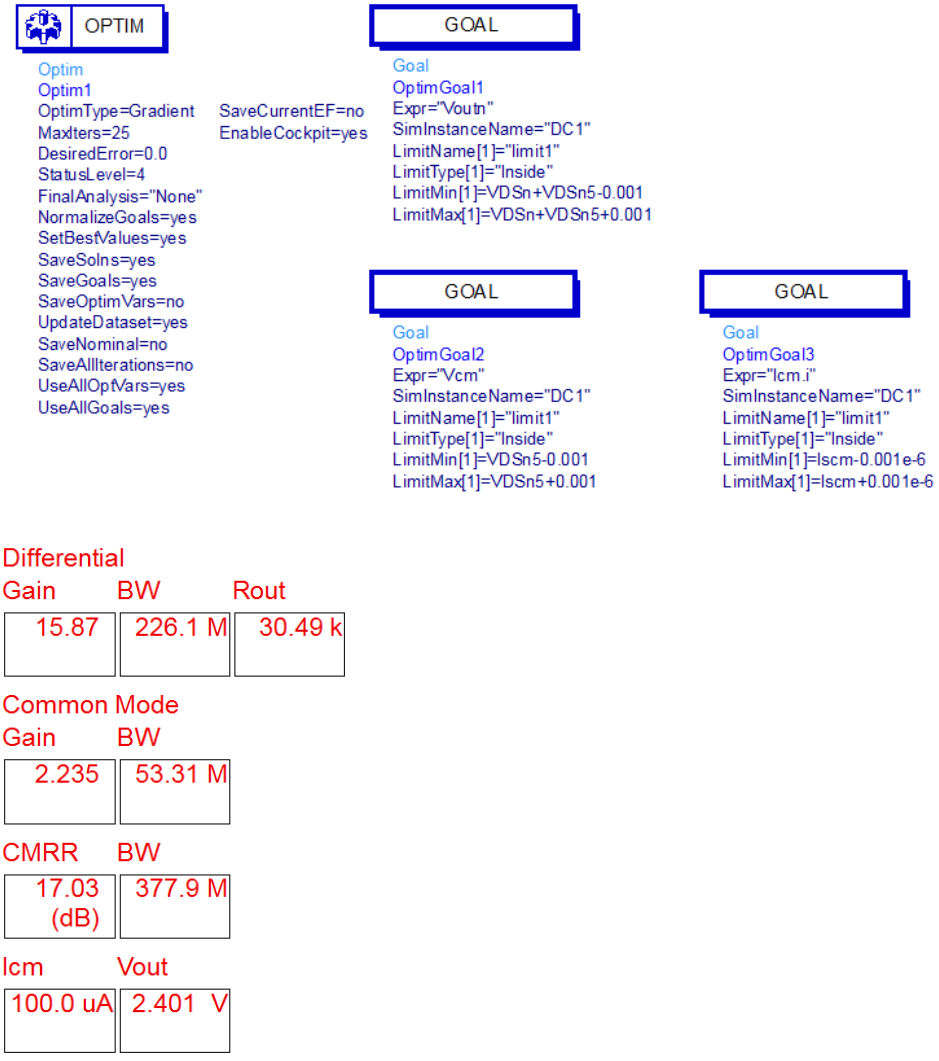



Figure 5-6 Optimization (Fine Tune) Setup and Results for Differential Amplifier

It is noteworthy that the simulated differential bandwidth and the CMMR bandwidth are determined at the point at which the differential voltage gain or CMMR have dropped -3dB from the low frequency gain (a.k.a. DC differential gain) or low frequency CMMR. The common mode bandwidth is considered to be the frequency at which the common mode voltage gain increases by +3dB. However we have observed that the common mode gain only exhibits this increase in the strong inversion region. In the weak and moderate inversion the common mode voltage gain may not increase at all at any frequency or may not reach the level of +3dB increase as seen in Figure 5-7. Clearly from the CM Gain plots in weak and moderate inversion a dominant pole in the frequency response has occurred before a dominant zero. Further investigation into this phenomenon is left as future research. For this dissertation we consider the common mode bandwidth infinite (INF) for those cases in which the +3dB frequency point does not exist. We note that the three bandwidths may not be the same and in fact the overall amplifier bandwidth will be dictated by the lower bandwidth among the three. In section 5.3 we show that for most of the frequency response versus inversion coefficient the differential bandwidth determines the overall bandwidth with the exception of strong inversion that is dominated by the CMRR bandwidth.

The common mode gain $A_{CM}$ of the differential amplifier deserves some further comments. The results in Figure 5-5 and Figure 5-6 show that $A_{CM} \approx 2.2$, which leads to a CMMR of only 17 dB. Notice that in Figure 5-2 all the channel lengths are set to the minimum channel length for this process, i.e. $L_{min}$=0.18 µm for the CA18HB TowerJazz process. The output resistance is directly proportional to the channel length and differential amplifier theory indicates [9, 10, and 11] that the higher the resistance of the

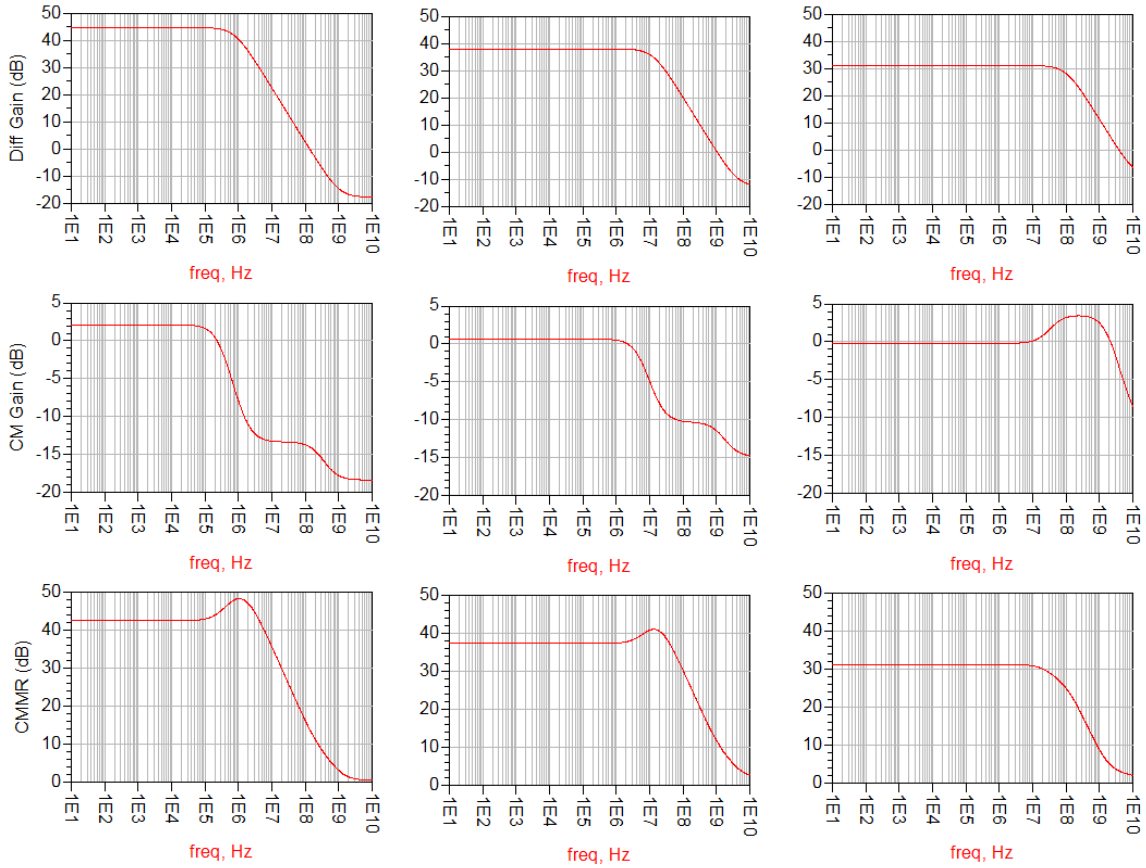



Figure 5-7 Differential Voltage Gain, Common Mode Gain and Common Mode Rejection Ratio for a Differential Amplifier with L=0.5 µm, 100 µA Tail Current (a) IC=0.1 (b) IC=1.0 (c) IC=10.0

tail current source the smaller the single ended $A_{CM}$ is, which can also be intuitively told from equation 5.3a. The higher $r_{ss}$ the lower $GM_{CM}$ is hence the lower $A_{CM}$. Improvement in the common mode gain can therefore be obtained by increasing the length of the tail current source NMOS transistor while not affecting the differential performance of the amplifier. An experiment was performed in which $A_{Diff}$ and $A_{CM}$ were measured for different L values of the NMOS tail current transistor as shown in Table 5-1. The results show that leaving the differential pair transistors M1 – M2 and the load transistors M3 –

M4 at their minimum length value while increasing the tail current NMOS transistor channel length (Lcm) reduces the common mode gain. Notice that just by increasing Lcm from 0.18 µm to 0.25 µm helps to reduce $A_{CM}$ by a factor of better than 2. The design setup of Figure 5-2 allows designers to easily make such tradeoffs in real time when moving the sliders.

Table 5-1 Differential Amplifier Tail Current Channel Length Increase - Experimental Results

| Ln (µm) | Lp (µm) | Lcm (µm) | $A_{Diff}$ | $A_{CM}$ | CMRR |
|---|---|---|---|---|---|
| 0.18 | 0.18 | 0.18 | 16.08 | 2.21 | 7.28 |
| 0.18 | 0.18 | 0.25 | 16.08 | 1.09 | 14.75 |
| 0.18 | 0.18 | 0.38 | 16.08 | 0.60 | 26.80 |
| 0.18 | 0.18 | 0.50 | 16.08 | 0.44 | 36.55 |
| 0.18 | 0.18 | 0.75 | 16.08 | 0.33 | 48.73 |
| 0.18 | 0.18 | 1.00 | 16.08 | 0.27 | 59.56 |

The simple differential amplifier of Figure 5-1 may prove not to be adequate for many applications in which a higher CMRR is desired. For such applications a more sophisticated tail current source implementation is needed. The design could very well be done with a cascode current source implementation. Further improvements to the basic differential amplifier are beyond the scope of our research.

## 5.3 Differential Amplifier Design Tradeoffs

Experiments similar to those done for the CS amplifier in section 4.7 are performed for the differential amplifier of Figure 5-1 as well. $V_{DD}$ is taken to be 3.6 V and each transistor is allocated a $V_{DS}$ = 1.2V. The bias current is set at 50µA for the differential pair. In this experiment three cases are studied as per Table 5-2. The Inversion Coefficients is set at 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, and 10. By using the slider setup

shown in Figure 5-2 the width values (W) and gate to source voltage ($V_{GS}$) values for all cases were determined and are shown in Table 5-3.

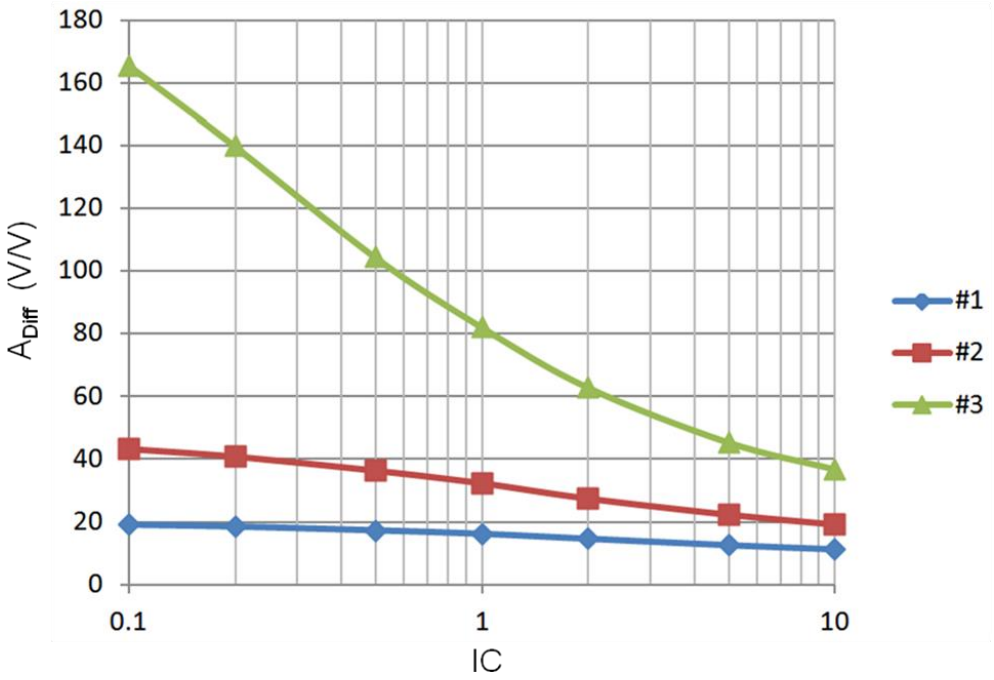
Table 5-2 Differential Amplifier Test Cases

| Test Case | $L_{NMOS1}$ (µm) | $L_{NMOS5}$ (µm) | $L_{PMOS}$ (µm) |
|---|---|---|---|
| #1 | 0.18 | 0.18 | 0.18 |
| #2 | 0.25 | 0.25 | 0.25 |
| #3 | 0.5 | 0.5 | 0.5 |

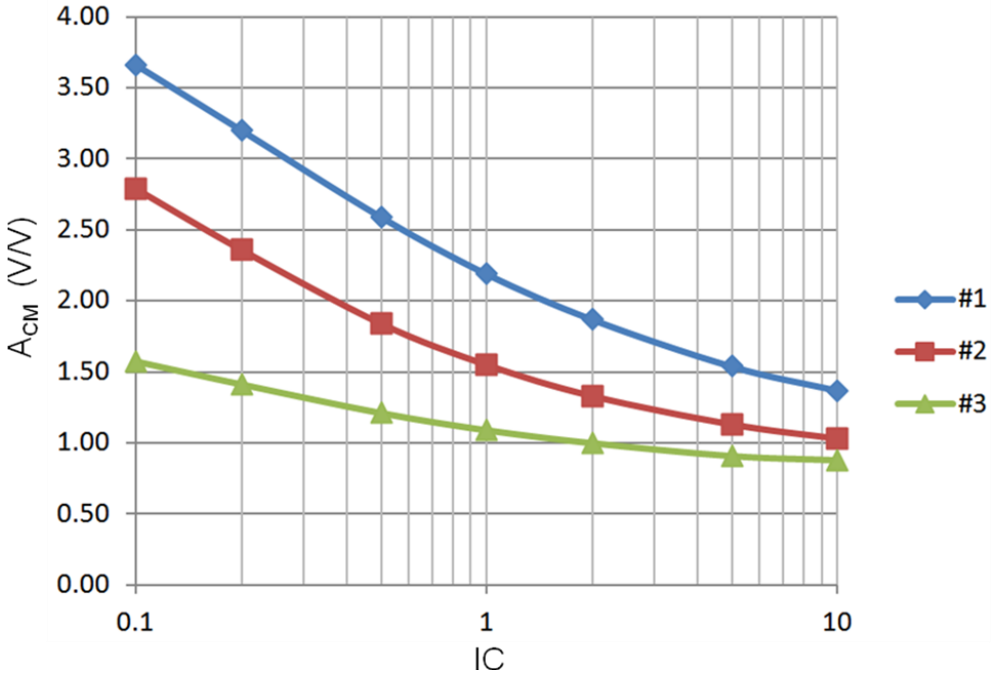
In the experiment the W and $V_{GS}$ values from Table 5-3 for all the test cases are then applied to build the schematic of Figure 5-4 in ADS. The designs are then analyzed to determine the small signal differential voltage gain, common mode gain, the value of the output resistance and the 3 dB bandwidth. Results for all these tests cases are shown graphically in Figure 5-8. These results follow the tradeoffs predicted by the MOS Operating Plane. The differential and common mode gains are both higher at the lower Inversion Coefficient (IC) levels. We notice that the CMMR does not follow any specific tradeoff (see Figure 5-8e). The values of CMMR become smaller as the channel length becomes smaller because $R_{out}$ of the tail current source is directly proportional to the channel length. The differential bandwidth (BW) increases with IC and is inversely proportional to the channel length. We have not included the common mode gain bandwidth within the results of our experiment as it resulted in an infinite value (i.e. there is no dominant zero). The only cases that exhibited any CM bandwidth occur for IC=10 (the edge of strong inversion) with bandwidth of 158.5 MHz, 71.78 MHz and 66.68 MHz for channel length of 0.18 µm, 0.25 µm and 0.5 µm respectively.

Table 5-3 Differential Amplifier Design Results

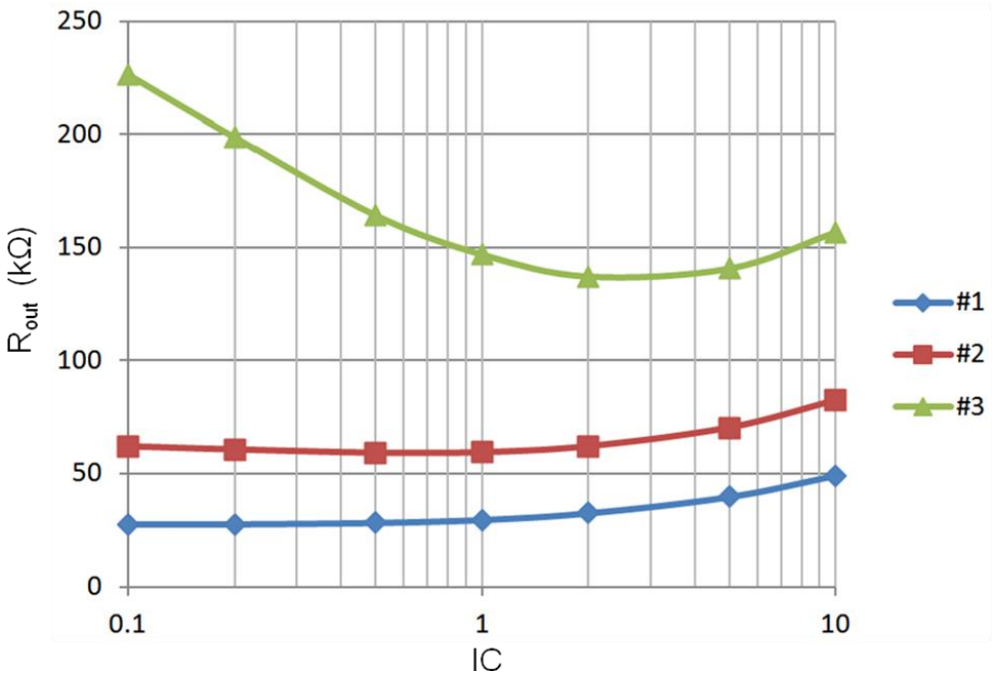
| $L_n$ = 0.18 µm<br>$L_p$ = 0.18 µm<br>$I_D$ = 50 µA<br>$V_{DD}$ = 3.6 V | | Case #1 | | | | |
|---|---|---|---|---|---|---|
| IC | Wn1 (µm) | Wn5 (µm) | Wp (µm) | VGSn (mV) | VGSn5 (mV) | VGSp (mV) |
| 0.1 | 180.01 | 321.72 | 457.24 | 533 | 366 | 362 |
| 0.2 | 90.01 | 160.86 | 228.62 | 560 | 392 | 387 |
| 0.5 | 36.00 | 64.34 | 91.45 | 595 | 430 | 422 |
| 1 | 18.00 | 32.17 | 45.72 | 621 | 463 | 451 |
| 2 | 9.00 | 16.09 | 22.86 | 660 | 501 | 485 |
| 5 | 3.60 | 6.43 | 9.14 | 723 | 567 | 546 |
| 10 | 1.80 | 3.22 | 4.57 | 790 | 635 | 615 |
| $L_n$ = 0.25 µm<br>$L_p$ = 0.25 µm<br>$I_D$ = 50 µA<br>$V_{DD}$ = 3.6 V | | Case #2 | | | | |
| IC | Wn1 (µm) | Wn5 (µm) | Wp (µm) | VGSn (mV) | VGSn5 (mV) | VGSp (mV) |
| 0.1 | 266.07 | 474.32 | 753.49 | 577 | 373 | 356 |
| 0.2 | 133.03 | 237.16 | 376.74 | 601 | 400 | 382 |
| 0.5 | 53.21 | 94.86 | 150.70 | 633 | 437 | 418 |
| 1 | 26.61 | 47.43 | 75.35 | 664 | 468 | 447 |
| 2 | 13.30 | 23.72 | 37.67 | 703 | 506 | 482 |
| 5 | 5.32 | 9.49 | 15.07 | 764 | 571 | 544 |
| 10 | 2.66 | 4.74 | 7.53 | 830 | 639 | 612 |
| $L_n$ = 0.5 µm<br>$L_p$ = 0.5 µm<br>$I_D$ = 50 µA<br>$V_{DD}$ = 3.6 V | | Case #3 | | | | |
| IC | Wn1 (µm) | Wn5 (µm) | Wp (µm) | VGSn (mV) | VGSn5 (mV) | VGSp (mV) |
| 0.1 | 568.05 | 996.21 | 1839.07 | 546 | 331 | 343 |
| 0.2 | 284.03 | 498.10 | 919.53 | 570 | 356 | 368 |
| 0.5 | 113.61 | 199.24 | 367.81 | 603 | 392 | 405 |
| 1 | 56.81 | 99.62 | 183.91 | 630 | 423 | 436 |
| 2 | 28.40 | 49.81 | 91.95 | 666 | 461 | 472 |
| 5 | 11.36 | 19.92 | 36.78 | 728 | 525 | 537 |
| 10 | 5.68 | 9.96 | 18.39 | 794 | 593 | 605 |


180
160
140
120
100
80
60
40
20
0
$A_{Diff}$ (V/V)
0.1
1
10
IC
#1
#2
#3

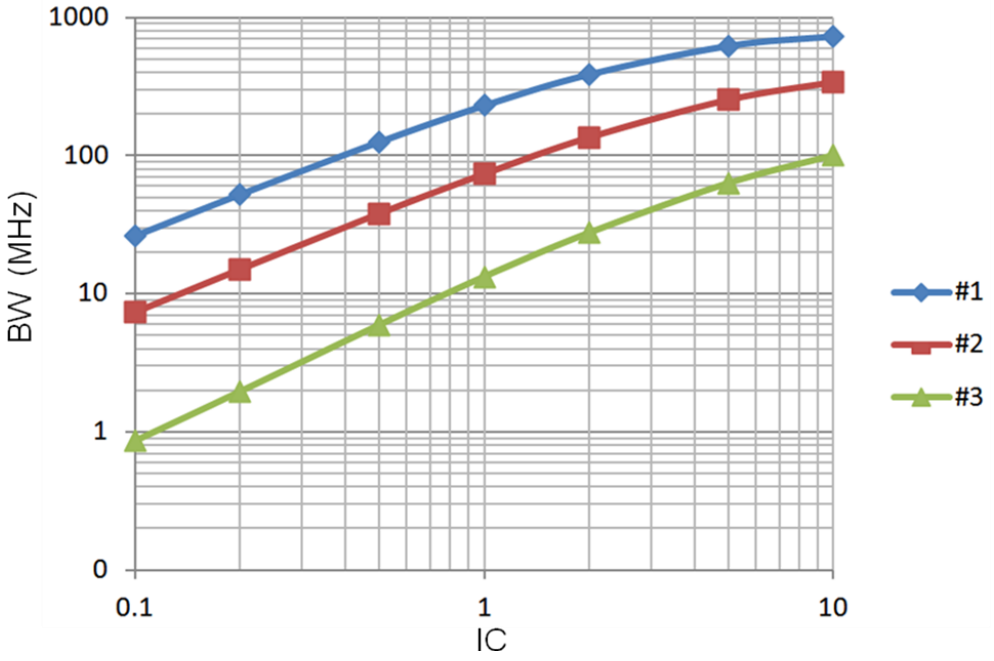
(a)


4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
$A_{CM}$ (V/V)
0.1
1
10
IC
#1
#2
#3

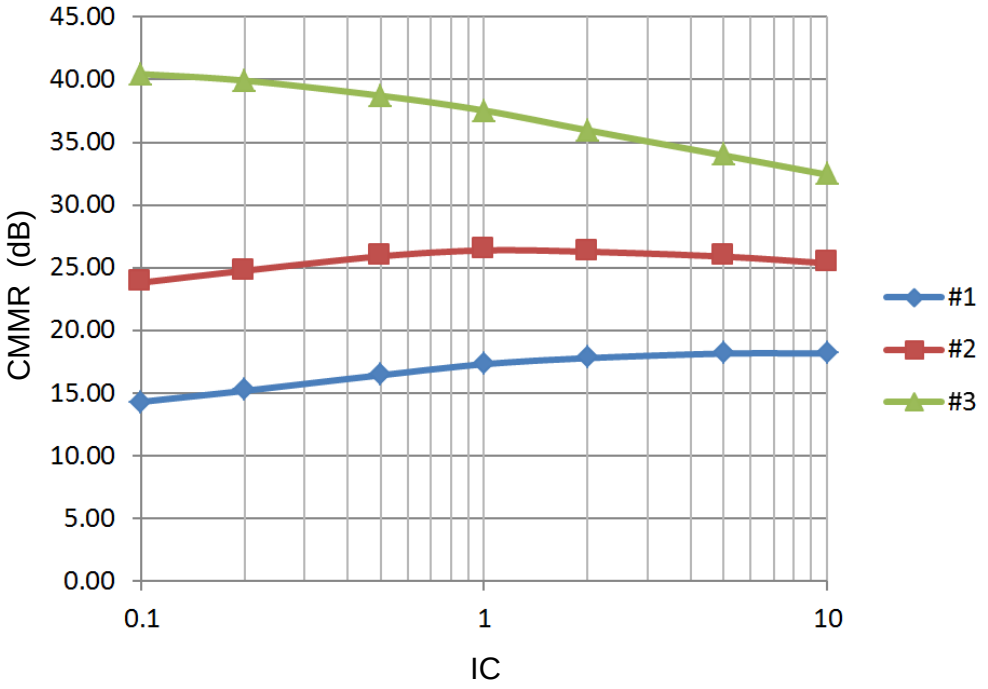
(b)


250
200
150
100
50
0
$R_{out}$ (kΩ)
0.1
1
10
IC
#1
#2
#3

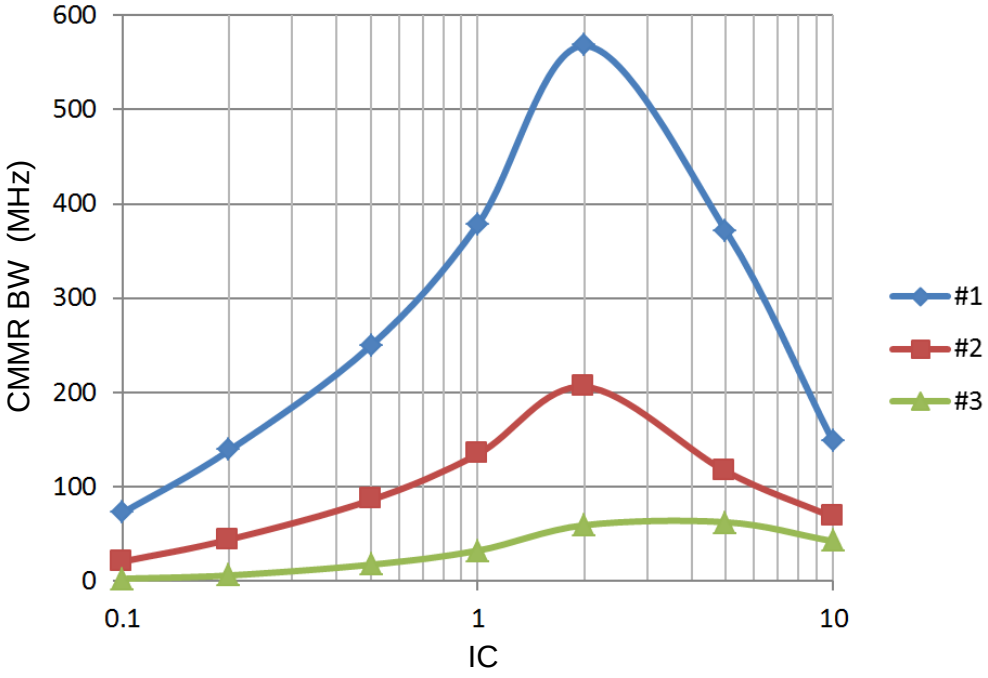
(c)


1000
100
10
1
0
BW (MHz)
0.1
1
10
IC
#1
#2
#3

(d)




(e)




(f)

Figure 5-8 Differential Amplifier Experiment Results (a) Differential Gain (b) Common Mode gain (c) Output Resistance (d) Differential Bandwidth (e) CMMR in dB (f) CMMR bandwidth

Summary of Differential Amplifier Experimental Results:

- The Differential Gain decreases with IC and increases with channel length (L)
- The Common Mode Gain decreases with IC and decreases with channel length (L) which is opposite to the differential gain behavior.
- The Output Resistance ($R_{out}$) results do not show any direct correlation with IC but it does clearly increase with channel length.
- The Differential Bandwidth increases with IC and decreases with L.
- The CMMR does not show any specific tradeoff versus IC but it increases with increasing the channel length.
- The CMMR bandwidth increases with IC up to the upper side of the moderate inversion and then it decreases the deeper one goes towards strong inversion. It decreases with an increase in the channel length.

These trends are very similar in nature to those of the single ended amplifiers and follow exactly trends predicted by Binkley's MOS Operating Plane. We have therefore shown that the MOS Operating Plane and the slider setup of Figure 5-2 can be used to design a Differential Amplifier with PMOS Current Load.

Whenever designing a differential amplifier one can observe from these tradeoffs that certain specifications may be easier to attain by modifying some of the initial selections made. For instance the designer may want to increase the differential gain, and for minor increases one may reduce the value of IC. However if one desire to increase the differential gain substantially and increase the CMRR as well, then it would be much easier to accomplish it by increasing the channel length first and then do fine tuning by

reducing the value of IC. For an increase in the bandwidth the tradeoffs are somewhat opposite, i.e. one would reduce the channel length and increase IC to increase the overall differential bandwidth but need to keep in mind that if IC moves into strong inversion the CMRR bandwidth dominates the overall amplifier bandwidth and it start dropping in value as IC increases.

## 5.4 Cascode Differential Amplifier

The cascode differential amplifier with PMOS cascode load (a.k.a. telescopic amplifier) is shown in Figure 5-9. Telescopic amplifiers provide higher gains since Rout is by several orders of magnitude larger than that of a simple differential amplifiers while essentially the same transconductance is obtained for similar bias conditions. The stacking of several MOSFET transistors makes biasing more challenging since less voltage ($V_{DS}$) is available for each transistor for the same fixed value of $V_{DD}$. The telescopic amplifier typically provides better bandwidth for those cases in which the source driving of the amplifier has finite resistance as this amplifier (similar to the single ended cascode) does not suffer as much from the Miller Effect. The gain for the cascode differential amplifier shown in Figure 5-9 can be derived from the knowledge gained from the basic amplifiers studied so far. We also take advantage of the MOS characterization that was needed for the prior three amplifiers study to create the slider setup. First we invoke the lemma [9] that in a linear circuit the voltage gain is equal to $G_M R_{OUT}$, where $G_M$ is the transconductance of the circuit and $R_{OUT}$ represents the output resistance of the circuit. Using this lemma the differential gain of the cascode differential amplifier is given by:

$$A_{Diff} = GM_{Diff} Rout_{Diff} \tag{5.9}$$

where $GM_{Diff}$ is the short circuit differential mode transconductance and $Rout_{Diff}$ is the differential mode output resistance. $GM_{Diff}$ is approximately equal to $g_{m1}$ (the transconductance of M1) as in the case of the single ended cascode, however due to the

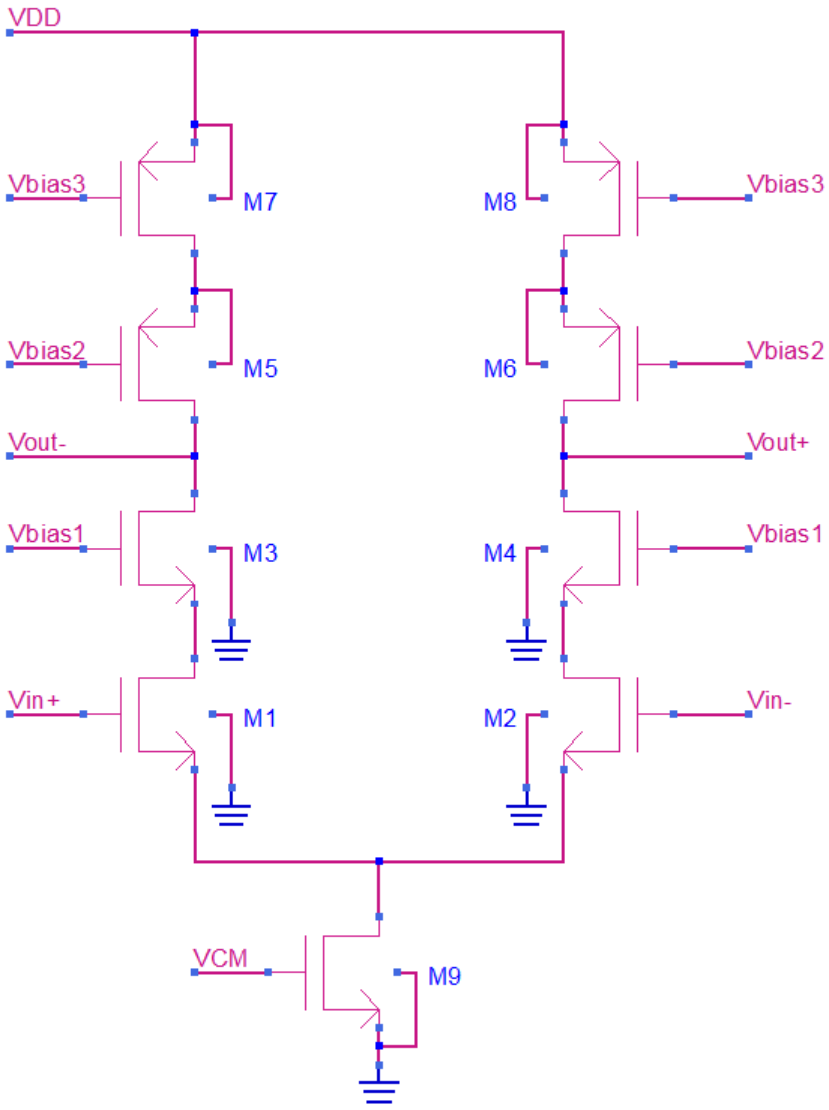



Figure 5-9 CMOS Cascode Differential Amplifier with Cascode PMOS Load

high gain values the cascode differential amplifier is capable of producing, we found it necessary to use the exact cascode transconductance expression [10]:

$$GM_{Diff} = g_{m1}\left(1 - \frac{1}{1 + (g_{m3} + g_{mb3})r_{o1} + \frac{r_{o1}}{r_{o3}}}\right) \tag{5.10}$$

The reason to include the extra $r_{o1}/r_{o3}$ term in (5.10) is because the value of the drain to source resistance ($r_o$) of the MOEFET becomes smaller with small channel length and hence the value of $r_{o1}/r_{o3}$ becomes significant when compared to $(g_{m3}+g_{mb3})r_{o1}$ This formula can be verified using the small-signal diagram [10, 33].

The differential transconductance efficiency of this amplifier can be expressed as:

$$\left(\frac{GM}{I_D}\right)_{Diff} = \left(\frac{g_m}{I_D}\right)_1\left(1 - \frac{1}{1 + \left(\frac{g_m + g_{mb}}{I_D}\right)_3\left(\frac{g_{ds}}{I_D}\right)_1^{-1} + \frac{g_{ds3}}{g_{ds1}}}\right) \tag{5.11}$$

Note that both $g_{ds3}$ and $g_{ds1}$ are normalized by $I_D$ but because these are at the same $I_D$ currents it cancels out so we do not show them normalized in the formula above, in the slider design setup the normalized values are of course used.

The differential output resistance is given by:

$$Rout_{Diff} = Rout_N \parallel Rout_P \tag{5.12}$$

where $Rout_N$ is the output resistance looking into the drain of M3 and $Rout_P$ is the output resistance looking into the drain of M5. Looking into the drain of M3 or M5 one "sees" the output resistance of a cascode amplifier and hence we can say:

$$Rout_N = (g_{m3} + g_{mb3})r_{o1}r_{o3} + r_{o1} + r_{o3} \tag{5.13}$$

$$Rout_P = (g_{m5} + g_{mb5}) r_{o7} r_{o5} + r_{o7} + r_{o5} \tag{5.14}$$

$$\left(\frac{gout}{I_D}\right)_N = \left[\left(\frac{g_m + g_{mb}}{I_D}\right)_3 \left(\frac{1}{\left(\frac{g_{ds}}{I_D}\right)_1 \left(\frac{g_{ds}}{I_D}\right)_3}\right) + \frac{1}{\left(\frac{g_{ds}}{I_D}\right)_1} + \frac{1}{\left(\frac{g_{ds}}{I_D}\right)_3}\right]^{-1} \tag{5.15}$$

$$\left(\frac{gout}{I_D}\right)_P = \left[\left(\frac{g_m + g_{mb}}{I_D}\right)_5 \left(\frac{1}{\left(\frac{g_{ds}}{I_D}\right)_7 \left(\frac{g_{ds}}{I_D}\right)_5}\right) + \frac{1}{\left(\frac{g_{ds}}{I_D}\right)_7} + \frac{1}{\left(\frac{g_{ds}}{I_D}\right)_5}\right]^{-1} \tag{5.16}$$

Taking the differential transconductance efficiency of (5.11) and the normalized conductances from (5.15) and (5.16) the cascode amplifier differential gain is finally expressed as:

$$A_{Diff} = \frac{\frac{GM_{Diff}}{I_D}}{\left(\left(\frac{g_{out}}{I_D}\right)_N + \left(\frac{g_{out}}{I_D}\right)_P\right)} \tag{5.17}$$

Equation (5.17) is the one implemented in the slider setup in ADS allowing an estimation of the differential gain based on selected points on the various curves.

Using the same voltage gain lemma the common mode gain is given by:

$$A_{CM} = GM_{CM} Rout_{CM} \tag{5.18}$$

where $GM_{CM}$ is the common mode transconductance and $Rout_{CM}$ is the common mode output resistance. The common mode transconductance of the cascode differential amplifier is the same as that of the differential amplifier of Figure 5-1 and is given by:

$$GM_{CM} = \frac{g_{m1}}{1+(g_{m1}+g_{mb1})r_{o9}+\frac{r_{o9}}{r_{ro1}}} \tag{5.19}$$

The common mode transconductance efficiency of this amplifier can be expressed as:

$$\left(\frac{GM}{I_D}\right)_{CM} = \frac{\left(\frac{g_m}{I_D}\right)_1}{1+\left(\frac{g_m+g_{mb}}{I_D}\right)_1\left(\frac{g_{ds}}{I_D}\right)_9^{-1}+\left(\frac{g_{ds}}{I_D}\right)_1\left(\frac{g_{ds}}{I_D}\right)_9^{-1}} \tag{5.20}$$

The common mode output resistance is given by:

$$Rout_{CM} = Rout_{CMN} \parallel Rout_p \tag{5.21}$$

Notice that for the common mode resistor the two PMOS transistors contribute the same resistance as in the differential mode, i.e. $Rout_P$ is as per equation (5.10). The output resistance contribution for the NMOS transistors i.e. looking into the drain of M3 is derived using a common source degenerated resistance approach. First one looks into the drain of M1 in common mode, notes that M1 is degenerated by the output resistance of M9 and this resistance is therefore given by [9, 10]:

$$Rout_{CM1} = (g_{m1}+g_{mb1})r_{o1}r_{o9}+r_{o1}+r_{o9} \tag{5.22}$$

Looking at M3 one notices that it is degenerated by $Rout_{CM1}$ and therefore the resistance looking into the drain of M3 in common mode is:

$$Rout_{CM2} = (g_{m3}+g_{mb3})r_{o3}Rout_{CM1}+r_{o3}+Rout_{CM1} \tag{5.23}$$

The current normalized conductances are:

$$\left(\frac{gout}{I_D}\right)_{CM1} = \left[\left(\frac{g_m+g_{mb}}{I_D}\right)_1\left(\frac{1}{\left(\frac{g_{ds}}{I_D}\right)_1\left(\frac{g_{ds}}{I_D}\right)_9}\right)+\frac{1}{\left(\frac{g_{ds}}{I_D}\right)_1}+\frac{1}{\left(\frac{g_{ds}}{I_D}\right)_9}\right]^{-1} \tag{5.24}$$

$$\left(\frac{gout}{I_D}\right)_{CMN} = \left[\left(\frac{g_m + g_{mb}}{I_D}\right)_3 \left(\frac{1}{\left(\frac{g_{out}}{I_D}\right)_{CM1}\left(\frac{g_{ds}}{I_D}\right)_3}\right) + \frac{1}{\left(\frac{g_{out}}{I_D}\right)_{CM1}} + \frac{1}{\left(\frac{g_{ds}}{I_D}\right)_3}\right]^{-1} \tag{5.25}$$

Using the common mode transconductance efficiency from (5.19) and the normalized conductances from (5.16) and (5.25) we expressed the cascode amplifier single ended common mode gain to be used in the slider setup as:

$$A_{CM} = \frac{\left(\frac{GM}{I_D}\right)_{CM}}{\left(\left(\frac{g_{out}}{I_D}\right)_{CMN} + \left(\frac{g_{out}}{I_D}\right)_P\right)} \tag{5.26}$$

## 5.5 Cascode Differential Amplifier Design

Design of the Cascode Differential amplifier of Figure 5-9 has been set up in ADS using the now familiar slider setup so that by moving a series of sliders the designer can track the impact of the design variable selections have on the amplifier differential gain, common mode gain and differential output resistance as shown in Figure 5-10. The slider setup takes advantage of the same process characterization that have been discussed for prior amplifiers so no new characterization is needed. The amplifier of Figure 5-9 requires that transistors M1 – M8 have the same $I_D$ with M9 having twice the current and therefore only one slider is needed for the current. The inversion coefficient is set for the entire amplifier where again in a strict sense this is not a hard requirement for this amplifier. $V_{DS}$ is set for each pair of transistors as follows: $V_{DS\_M1}$=$V_{DS\_M2}$, $V_{DS\_M3}$=$V_{DS\_M4}$, $V_{DS\_M5}$=$V_{DS\_M6}$, $V_{DS\_M7}$=$V_{DS\_M8}$. The channel length can be set up individually for each pair of transistors as is done for $V_{DS}$ but we chose to let L for the

NMOS and PMOS transistors in the amplifier have the same length and the length of the current source transistor is set separately as shown in the slider setup of Figure 5-10. This amplifier also has a DC voltage restriction that must be accommodated by the slider

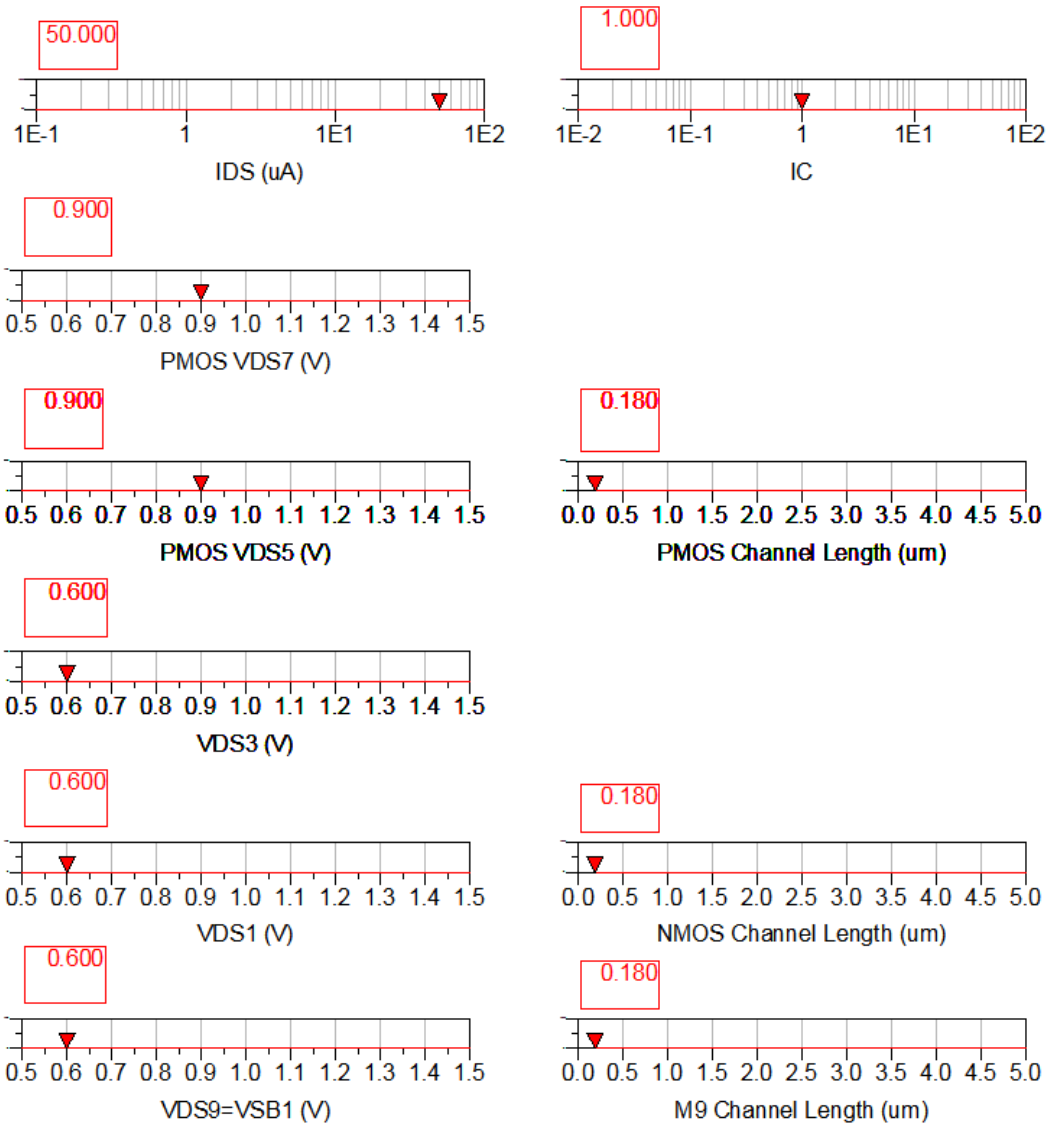



Figure 5-10 Cascode Differential Amplifier Design – Sliders Setup

design setup. Analysis of Figure 5-9 shows that the drain to source voltage ($V_{DS}$) of M9 is the Source to Bulk ($V_{SB}$) voltage of M1 (M2) and that $V_{DS9}+V_{DS1} = V_{SB3}$. Therefore

when selecting $g_m/I_D$ and $g_{ds}/I_D$ for M3 we set $V_{SB\text{-}M3} = V_{DS\text{-}M1} + V_{DS\text{-}M9}$ and for M1 by setting $V_{SB\text{-}M1} = V_{DS\text{-}M9}$. This is a clear indication that for the same $V_{DD}$ the bias of the cascode differential amplifier is more challenging and results in reduced voltage headroom for the signal being amplified when compared to the differential amplifier of Figure 5-1.

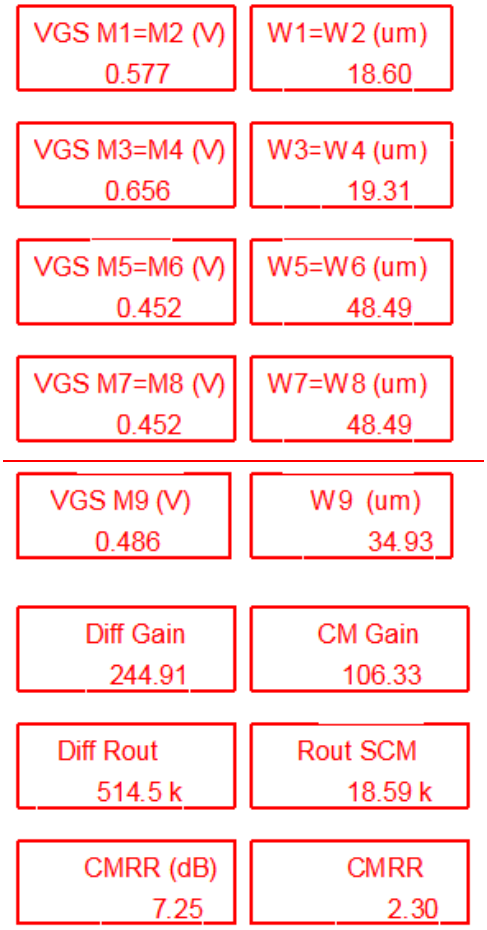



Figure 5-11 Cascode Differential Amplifier Design Parameters, Gain and Output Resistance

The design from the slider setup shown in Figure 5-11 is then captured in ADS to verify our design methodology. The design setup is very similar as that for the differential amplifier shown in Figure 5-4. The results of this simulation are shown in

Figure 5-12. Notice that we expect the tail current to be 100 µA and the results show Icm=96.20 µA which we consider is acceptable and within round-off error however the output DC voltage is significantly below the 1.8 V expected. These two errors are enough to result in an amplifier which has significantly different values than those from Figure 4-10. The differences can be corrected by some fine tuning which we decided to do using an optimizer similar to the one shown in Figure 5-6. The optimizable variables are the $V_{GS}$ voltages for the MOS transistors and we allowed a range from 0.2 V to 1.5 V. We remind the reader that this optimization is invoked to make sure that the DC bias is consistent and it is similar in action to creating a DC feedback design to stabilize the DC circuit. The results feature very small corrections (a few mV at most) for each voltage.

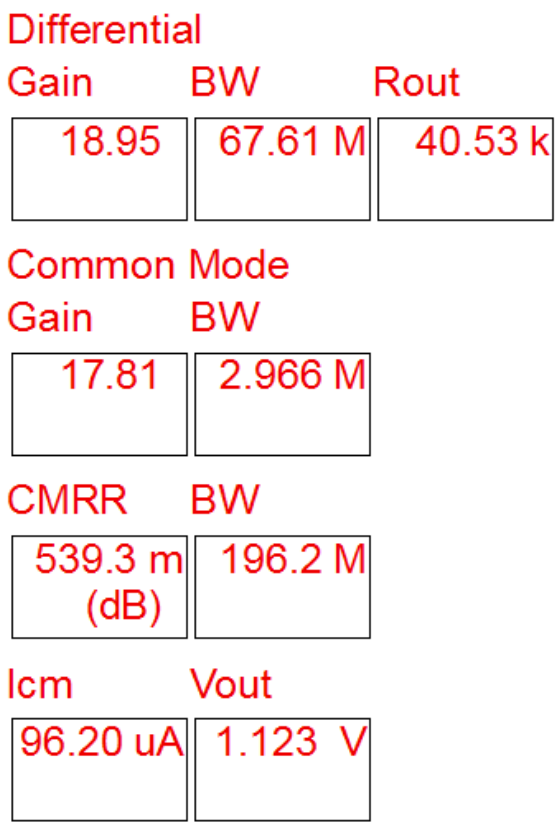



Figure 5-12 Results of Simulation for Cacode Differential Amplifier

The fine-tuned $A_{Diff}$, $R_{out}$ and $A_{CM}$ did result in a significant change compared to our original simulation as shown in Figure 5-13. In this case the optimizer provided significant improvements to the drain to source voltages and currents so that these match the design values which is an indication that this amplifier is very sensitive to small changes in the bias voltages

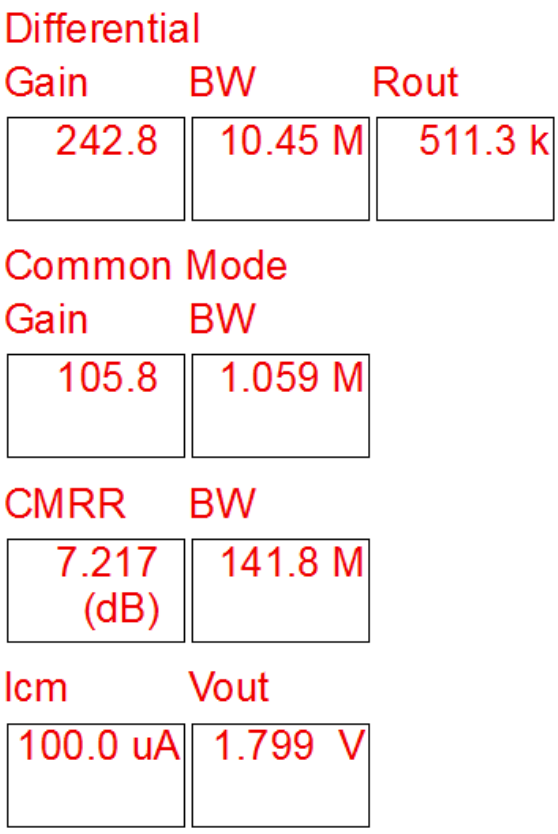



Figure 5-13 Optimization (Fine Tune) Results for Cascode Differential Amplifier

## 5.6 Cascode Differential Amplifier Tradeoffs

Experiments similar to those done for the differential amplifier in section 5.3 are also performed for the cascode differential amplifier of Figure 5-9. The $V_{DD}$ used is 3.6 V

and we allocate 0.6 V for each NMOS transistor and 0.9 V for each PMOS transistor drain to source voltage. Bias current is set at 50µA for the differential pair. In this experiment three cases are studied as per Table 5-4. The Inversion Coefficients will be set at 0.1, 0.2, 0.5, 1.0, 2.0, 5.0, and 10, which is a very good sampling from weak inversion to strong inversion. Using the slider setup shown in Figure 5-10 the width values (W) and gate to source voltage ($V_{GS}$) values for all cases were determine and are shown in Table 5-5.

Table 5-4 CascodeDifferential Amplifier Test Cases

| Test Case | $L_{NMOS}$ (µm) | $L_{NMOS9}$ (µm) | $L_{PMOS}$ (µm) |
|---|---|---|---|
| #1 | 0.18 | 0.18 | 0.18 |
| #2 | 0.25 | 0.25 | 0.25 |
| #3 | 0.5 | 0.5 | 0.5 |

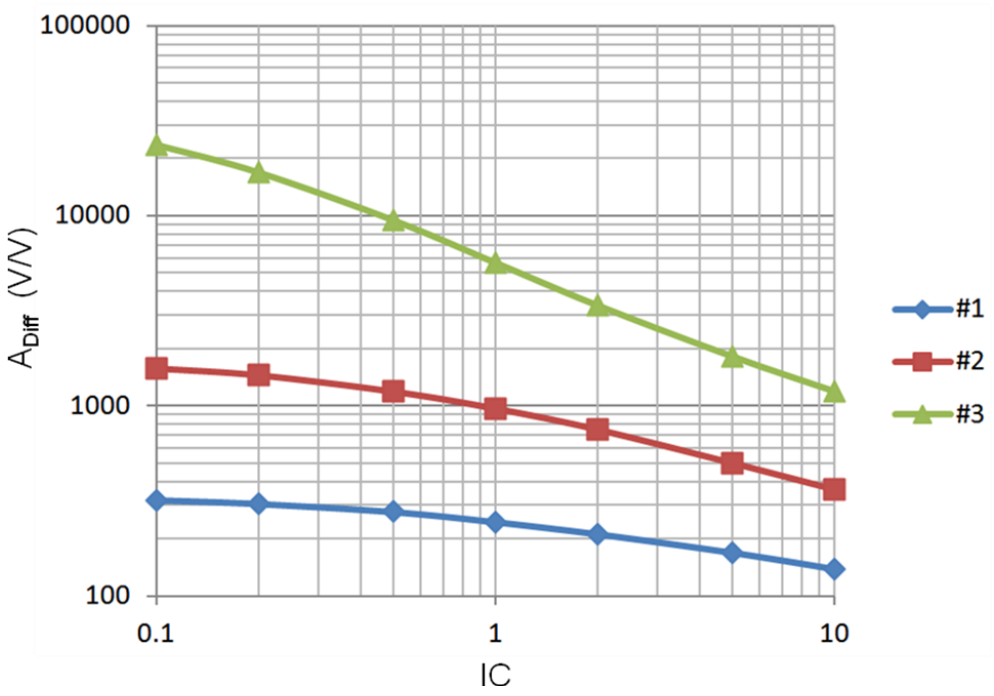
In the experiment the W and $V_{GS}$ values from Table 5-5 for all the test cases are then use to build the schematic in ADS. The designs are then analyzed to determine the small signal differential voltage gain, common mode gain, the value of the output resistance and the 3 dB bandwidth. Results for all tests cases are shown graphically in Figure 5-14. Test cases 1, 2 & 3 differ mainly by the size of the channel length used which is the same for all the MOS devices in each test.

Summary of Telescopic Amplifier Experiment Results:

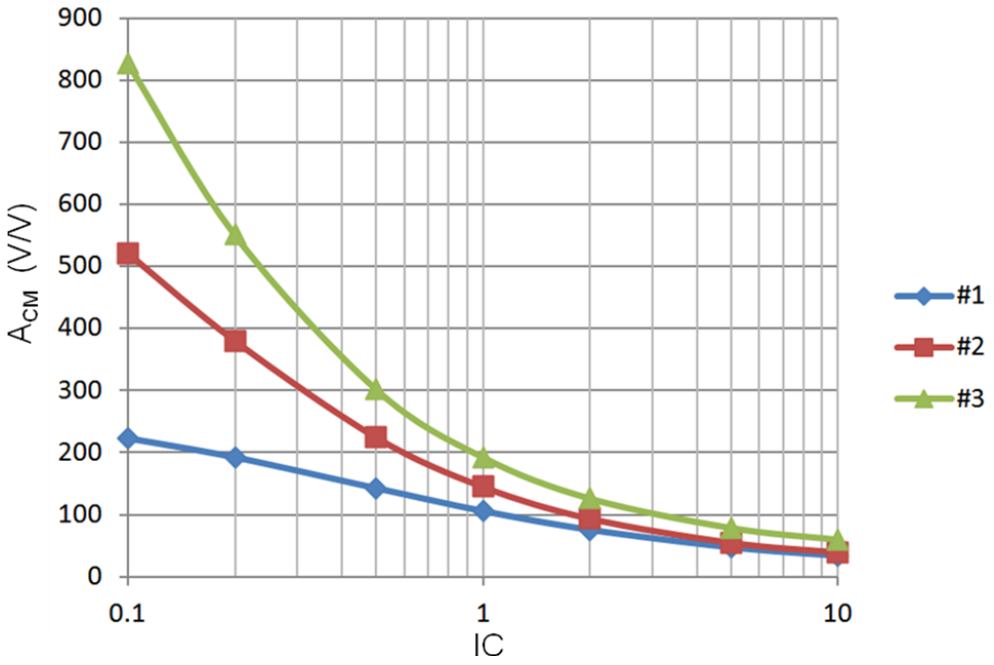
- The Differential Gain decreases with IC and increases with channel length (L) and is significantly larger than for the differential amplifier
- The Common Mode Gain decreases with IC and increases with channel length (L)

Table 5-5 Cascode Differential Amplifier Design Results

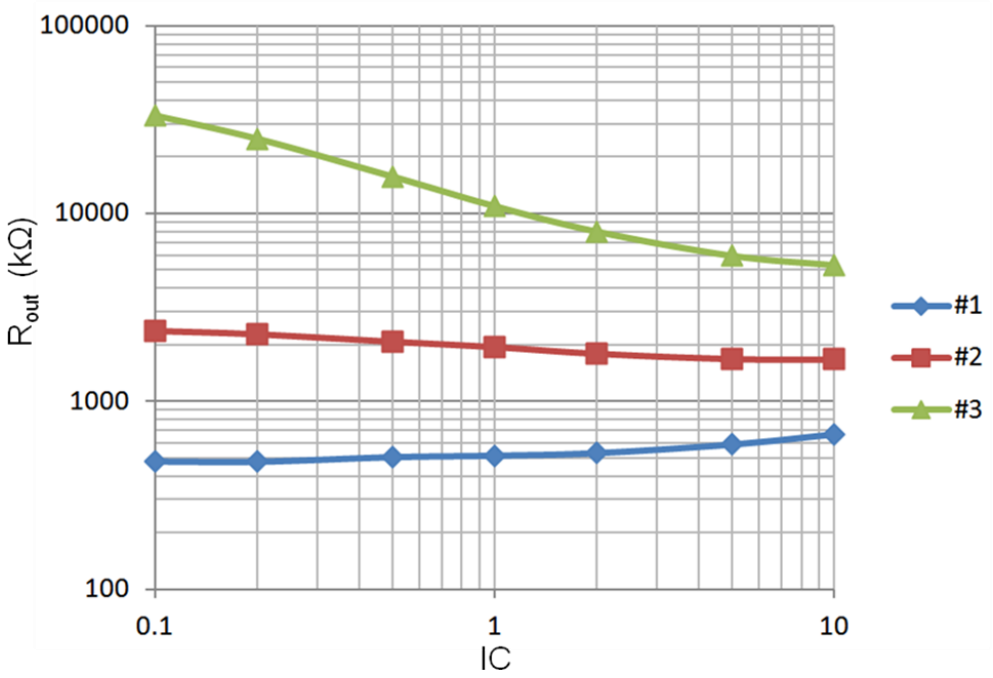
| $L_n$ = 0.18 µm<br>$L_p$ = 0.18 µm<br>$I_D$ = 50 µA<br>$V_{DD}$ = 3.6 V | Case #1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| IC | Wn1 (µm) | Wn3 (µm) | Wp (µm) | Wn9 (µm) | VGSn (mV) | VGSn3 (mV) | VGSp (mV) | VGSn9 (mV) |
| 0.1 | 186.04 | 193.07 | 484.89 | 349.30 | 481 | 563 | 362 | 387 |
| 0.2 | 93.02 | 96.53 | 242.44 | 174.65 | 506 | 589 | 387 | 414 |
| 0.5 | 37.21 | 38.61 | 96.98 | 69.86 | 544 | 621 | 423 | 453 |
| 1 | 18.60 | 19.31 | 48.49 | 34.93 | 577 | 656 | 452 | 486 |
| 2 | 9.30 | 9.65 | 24.24 | 17.46 | 613 | 695 | 487 | 526 |
| 5 | 3.72 | 3.86 | 9.70 | 6.99 | 678 | 759 | 549 | 593 |
| 10 | 1.86 | 1.93 | 4.85 | 3.49 | 748 | 826 | 618 | 662 |
| $L_n$ = 0.25 µm<br>$L_p$ = 0.25 µm<br>$I_D$ = 50 µA<br>$V_{DD}$ = 3.6 V | Case #2 | | | | | | | |
| IC | Wn1 (µm) | Wn3 (µm) | Wp (µm) | Wn9 (µm) | VGSn (mV) | VGSn3 (mV) | VGSp (mV) | VGSn9 (mV) |
| 0.1 | 270.81 | 283.12 | 787.86 | 504.60 | 490 | 588 | 356 | 382 |
| 0.2 | 135.41 | 141.56 | 393.93 | 252.30 | 516 | 609 | 382 | 408 |
| 0.5 | 54.16 | 56.62 | 157.57 | 100.92 | 553 | 651 | 418 | 446 |
| 1 | 27.08 | 28.31 | 78.79 | 50.46 | 585 | 677 | 448 | 479 |
| 2 | 13.54 | 14.16 | 39.39 | 25.23 | 619 | 716 | 483 | 518 |
| 5 | 5.42 | 5.66 | 15.76 | 10.09 | 685 | 780 | 546 | 584 |
| 10 | 2.71 | 2.83 | 7.88 | 5.05 | 754 | 848 | 614 | 653 |
| $L_n$ = 0.5 µm<br>$L_p$ = 0.5 µm<br>$I_D$ = 50 µA<br>$V_{DD}$ = 3.6 V | Case #3 | | | | | | | |
| IC | Wn1 (µm) | Wn3 (µm) | Wp (µm) | Wn9 (µm) | VGSn (mV) | VGSn3 (mV) | VGSp (mV) | VGSn9 (mV) |
| 0.1 | 562.73 | 594.08 | 1875.15 | 1036.83 | 445 | 547 | 343 | 332 |
| 0.2 | 281.36 | 297.04 | 937.58 | 518.42 | 470 | 572 | 368 | 358 |
| 0.5 | 112.55 | 118.82 | 375.03 | 207.37 | 506 | 605 | 406 | 395 |
| 1 | 56.27 | 59.41 | 187.52 | 103.68 | 537 | 634 | 437 | 427 |
| 2 | 28.14 | 29.70 | 93.76 | 51.84 | 574 | 671 | 474 | 465 |
| 5 | 11.25 | 11.88 | 37.50 | 20.74 | 636 | 735 | 539 | 531 |
| 10 | 5.63 | 5.94 | 18.75 | 10.37 | 703 | 801 | 607 | 600 |


100000
10000
1000
100
$A_{Diff}$ (V/V)
0.1
1
10
IC
#1
#2
#3

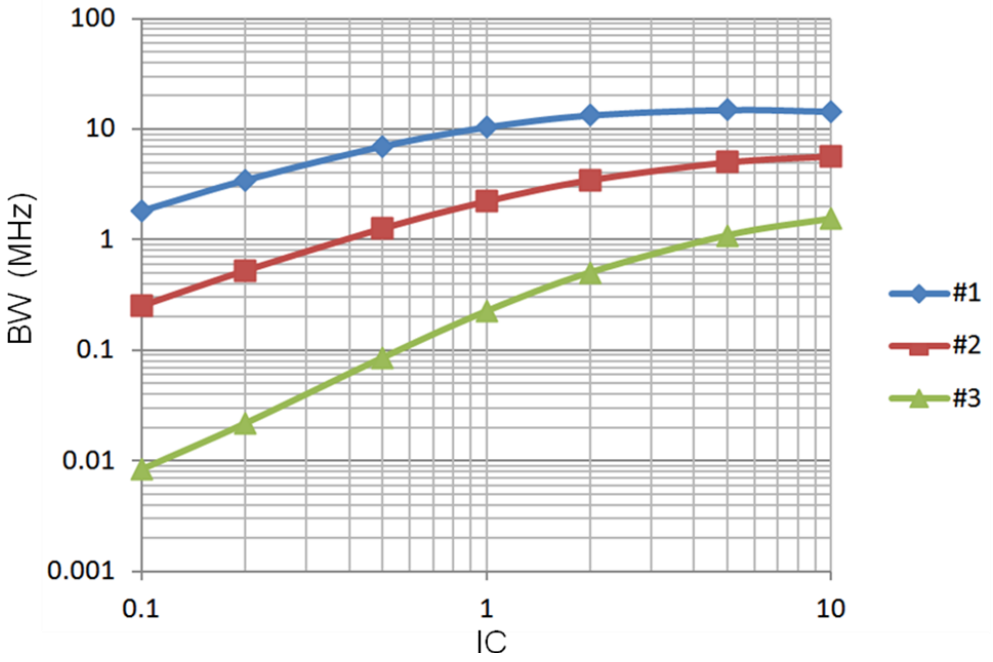
(a)


900
800
700
600
500
400
300
200
100
0
$A_{CM}$ (V/V)
0.1
1
10
IC
#1
#2
#3

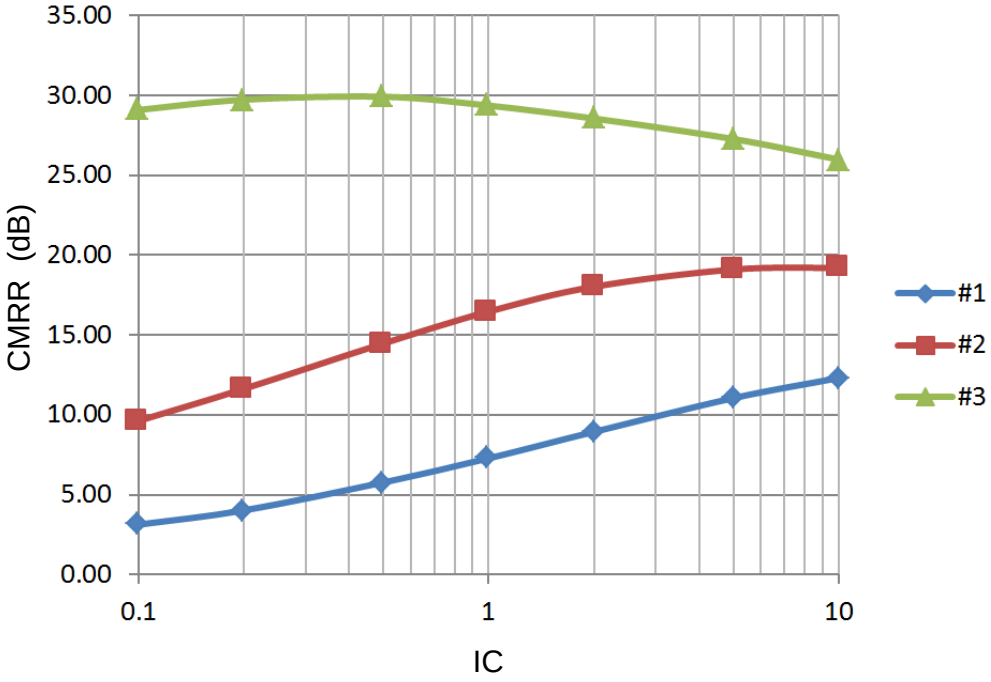
(b)


100000
10000
1000
100
$R_{out}$ (kΩ)
0.1
1
10
IC
#1
#2
#3

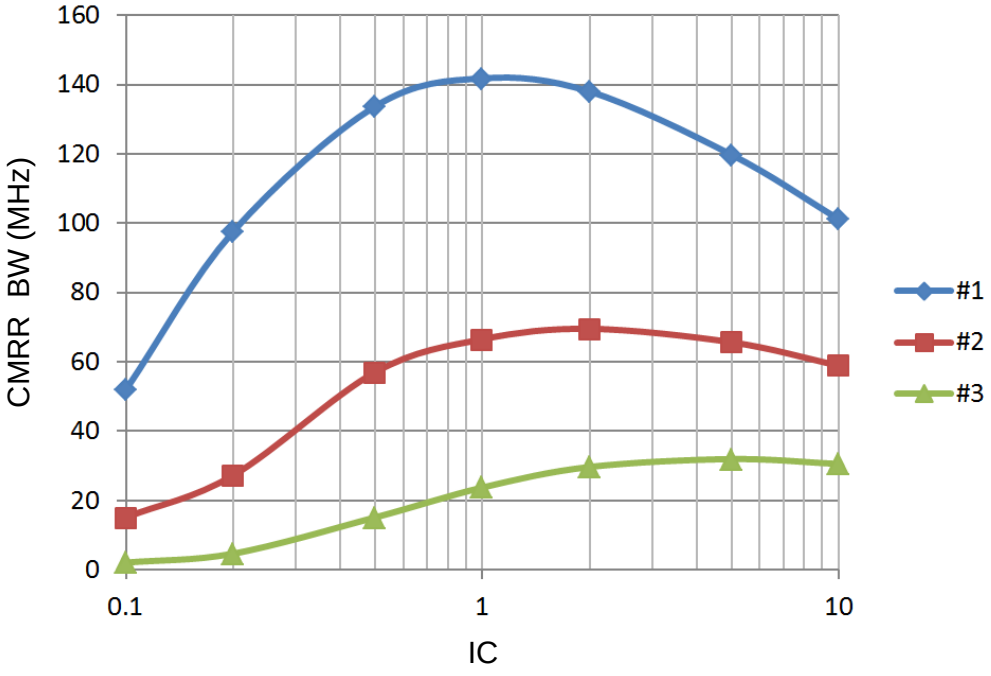
(c)


100
10
1
0.1
0.01
0.001
BW (MHz)
0.1
1
10
IC
#1
#2
#3

(d)




(e)




(f)

Figure 5-14 Cascode Differential Amplifier Experiment Results (a) Differential Gain (b) Common Mode gain (c) Output Resistance (d) Differential Bandwidth (e) CMMR in dB (f) CMMR bandwidth

- The Output resistance ($R_{out}$) results do not show any direct correlation with IC but it does clearly increase with channel length and is significantly larger than for the differential amplifier due to cascoding.
- The differential bandwidth increases with IC and decreases with L and is significantly smaller than for the differential amplifier. Test were done with zero resistance ideal voltage source if a finite resistance voltage source were used then we expect the Cascode differential amplifier to have better bandwidth because the Cascode amplifier does not suffer from Miller Effect.
- The Common Mode bandwidth for all cases tested was infinite, i.e. we did not encounter any with a dominant zero.
- The common mode rejection ratio (CMRR) increase with L and is a weak function of the IC.
- The CMRR bandwidth increases as L decreases and increases from weak to moderate inversion but as we approach the strong inversion region it decreases.

These tradeoffs are very similar in nature to those of the other amplifiers studied in this dissertation and follow exactly the tradeoffs predicted by Binkley's MOS Operating Plane. We have therefore shown that the MOS Operating Plane and the slider setup of Figure 5-9 can be used to design a Cascode Differential Amplifiers with Cascode PMOS Current Load.

Comparing the performance of the Differential Amplifier with PMOS Current Load to that of the Cascode Differentail Amplifier we notice that the differential gain of the latter can be anywhere from 5 times greater at L=0.18 μm to as much as hundred-fold

larger for L=0.5 μm. In terms of the CMRR the simple Differential Amplifier outperformed the Cascode Differential Amplifier which may give the reader the impression that the former is a better amplifier however we restricted ourselves to a simplistic tail current source. If an improved tail current source (perhaps cascoded) were used the Cascode Differential Amplifier will most likely outperform the simpler version. As far as the bandwidth trends of the two differential amplifiers we leave as future research. Future research into this matter must consider that the actual usable bandwidth depends on the differential, common mode and CMMR frequency responses and Miller's effect of these amplifiers.

# 6.0 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

## 6.1 Simple OTA

The simple OTA of Figure 6-1 can also be designed using the same techniques shown for the amplifiers of chapter 4 and 5. There are many different types of OTA design circuits we chose this particular one in order to compare results to those in [3, 7]. The design procedures and results from these references will serve as a benchmark for our methodologies.

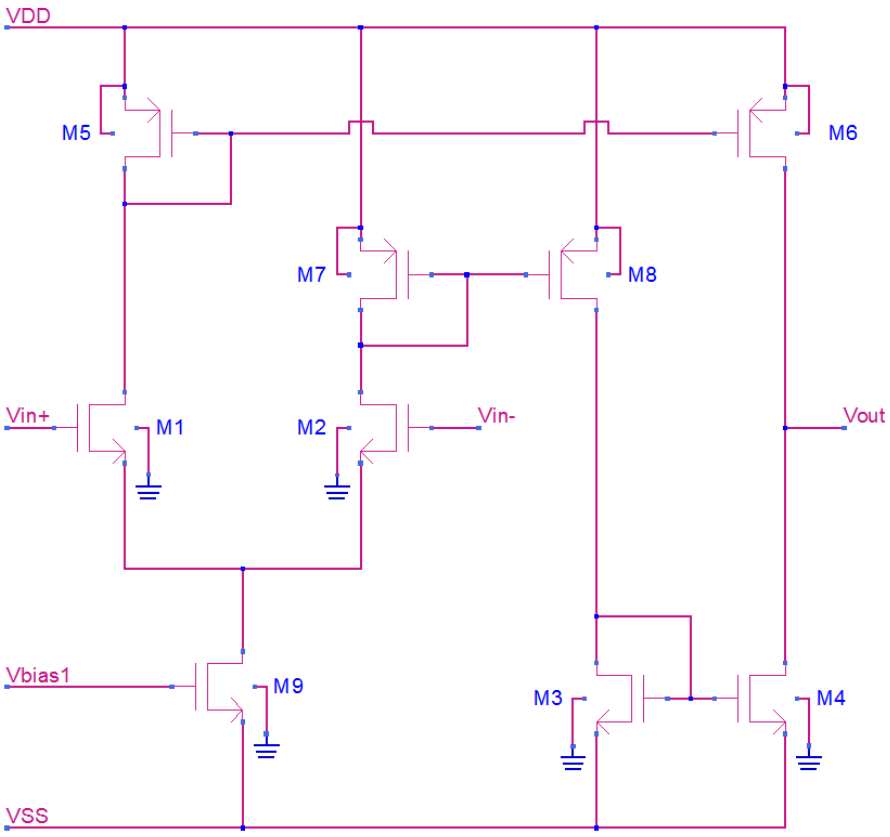



Figure 6-1 Simple Operational Transconductance Amplifier (OTA)

A differential pair formed by M1 and M2 with PMOS diode connected transistor loads (M5 and M7) form the input of the OTA. Diode connected transistors M5 and M7 form a current mirror with transistors M6 and M8. The current from M8 is then steered to NMOS transistor M3 which forms another current mirror with M4. Transistors M4 and M6 are the complementary single ended output transistors. We note that this simple OTA may not meet the high output resistance needed in many OTA applications. However the design techniques and issues studied are generic to all OTAs.

The simple OTA of Figure 6-1 has some specific biasing requirements that we have not seen in any of the amplifiers studied earlier in this thesis. Obviously since M1 = M2 and M5 = M7 the bias conditions of these pairs of transistors must be equal to keep the differential amplifier balanced. Transistors M5 and M7 are in a diode connected configuration therefore when creating the ADS slider setup one must make sure that $V_{GS}$ = $V_{DS}$ for both transistors as well. This latest requirement may seem a trivial matter at first but since $V_{GS}$ controls the IC value, then as one moves the sliders one must constantly also change $V_{DS}$ to match. Note that the same applies to transistor M3. Our design is different from [7] as we decided to use a dual supply approach in order to study and design a zero DC offset output OTA. Other bias conditions that are needed for the simple OTA are:

$$V_{SB1} = V_{DS9} \tag{6.1}$$

$$V_{DD} + V_{SS} = V_{DS9} + V_{DS1} + V_{DS5} = V_{DS3} + V_{DS8} = V_{DS4} + V_{DS6} \tag{6.2}$$

$$V_{GS5} = V_{GS6} \tag{6.3}$$

$$V_{GS7} = V_{GS8} \tag{6.4}$$

Furthermore if zero DC offset is required then:

$$V_{DS3} = V_{DS8} = V_{DS4} = V_{DS6} \tag{6.5}$$

An approximated transconductance expression of the simple OTA is given by [7]:

$$GM_{OTA} = g_{m_1} = \left(\frac{g_m}{I_D}\right)_1 \cdot I_{D1} \tag{6.6}$$

where $I_{D1}$ is the drain current of M1.

This expression excludes the loss of signal due to the loading by the device drain to source resistances ($r_{ds}$) of the load diode connected transistors M5 and M7. In this thesis we decided to incorporate these effects in the calculations of $GM_{OTA}$ because as the devices get smaller the reduction in the value of $r_{ds}$ makes this impact a significant amount. The corrected expression for the transconductance is:

$$GM_{OTA} = g_{m_1}\left(\frac{r_{ds1}}{r_{ds1} + r_{ds5}}\right) = \left(\frac{g_m}{I_D}\right)_1 \left(\frac{\left(\frac{g_{ds}}{I_D}\right)_5}{\left(\frac{g_{ds}}{I_D}\right)_1 + \left(\frac{g_{ds}}{I_D}\right)_5}\right) I_{D1} \tag{6.7}$$

Furthermore $GM_{OTA}$ can be adjusted by adjusting the current mirror gain factor ($K_i$) that was assumed $K_i$=1 in equation (6.6). The final expression is then given by:

$$GM_{OTA} = K_i\left(\frac{g_m}{I_D}\right)_1 \left(\frac{\left(\frac{g_{ds}}{I_D}\right)_5}{\left(\frac{g_{ds}}{I_D}\right)_1 + \left(\frac{g_{ds}}{I_D}\right)_5}\right) I_{D1} \tag{6.8}$$

The output resistance of the simple OTA is given by:

$$R_{Out} = r_{ds4} \parallel r_{ds6} = \frac{1}{g_{ds4} + g_{ds6}} = \left( \frac{1}{\left(\frac{g_{ds}}{I_D}\right)_4 + \left(\frac{g_{ds}}{I_D}\right)_6} \right) \frac{1}{K_i I_{D1}} \tag{6.9}$$

## 6.2 Simple Operational Transconductance Amplifier Design

Design of the simple OTA of Figure 6-1 has been set up in ADS similar to what was done for the other amplifiers. The needed current normalized conductance and transconductance efficiency curves for each transistor are selected based on the $V_{DS}$, L and $V_{SB}$ (if needed) and then equations (6.8) and (6.9) are used to determine the OTA performance. Moving a series of sliders as seen in Figure 6-2 the designer can immediately see the impact of the design variable selections has on the OTA transconductance and output resistance as shown in Figure 6-3. The currents slider is for the current of the differential pair transistors with the current through M3, M4, M6 and M8 set to Kfac*IDS. The channel length is controlled by transistor type, i.e. there is one slider for the NMOS transistors and one for the PMOS transistors. Notice that there are five $V_{DS}$ voltages in this setup. This large number of sliders is needed to satisfy the requirements of equation (6.2), this is of the upmost importance since the prediction of $GM_{OTA}$ and $R_{OUT}$ are dependent on the correct $V_{DD}$+$V_{SS}$ and the individual transistors $V_{DS}$ values. The reader will also notice that we have two sliders for the inversion coefficient, for now we will just leave them at the same value. We explain below the need for a second IC slider.

The design results in Figure 6-3 was a results of moving the sliders to obtain a desired GM = 1mA/V. We started the design with a $V_{DD}+V_{SS}=2V$, an IC level system requirement which makes sense since this makes the $V_{DS}$ and $V_{GS}$ voltage values in the range of values allowed for this process. This imposes restrictions on the transistor $V_{DS}$ voltages as per (6.2). Once the $V_{DS}$ of all the transistors are selected some adjustment is possible but always obeying the restrictions of (6.2). After the $V_{DS}$ voltages have been

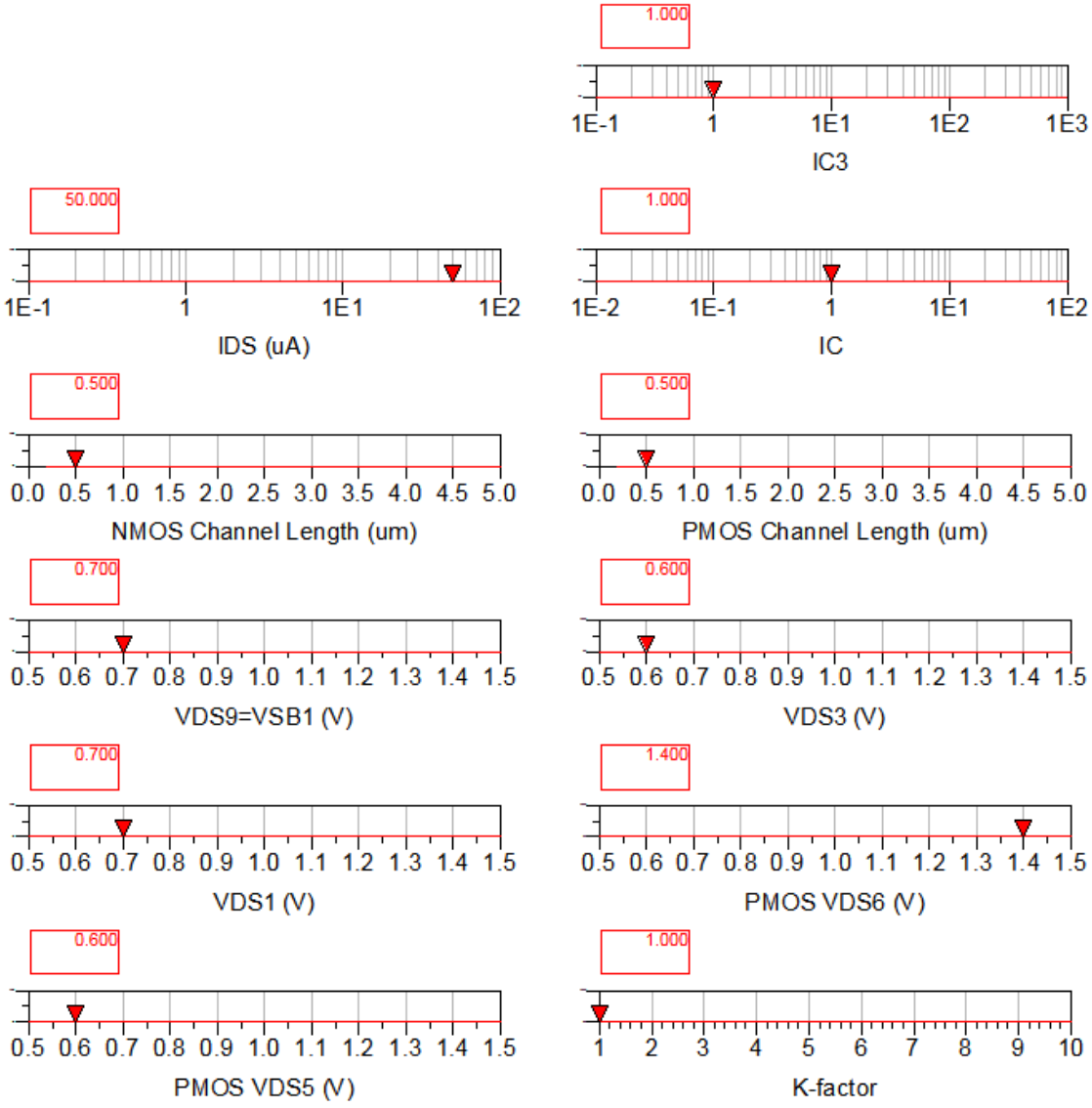



Figure 6-2 Simple Operational Transconductance Amplifier Design – Sliders Setup

selected then the user can modify either the channel length, IC or Kfac to meet the requirements. For example the user may choose to increase the value of Kfac which in turn increases the current at the output transistors which increases the width of these transistors and reduces the output resistance. During testing of the OTA frequency response one may find that the bandwidth is too low then one may return to the slider and reduce the Kfac and instead reduce the IC in order to increase the GM of the OTA back to meet the requirement, this will in effect increase the width of the differential amplifier but will not impact the OTA frequency response since the BW of the OTA is determined by the output transistors. This simple experiment shows us that the value of Kfac is to be chosen carefully as increasing it does have a negative impact on the bandwidth and output resistance.

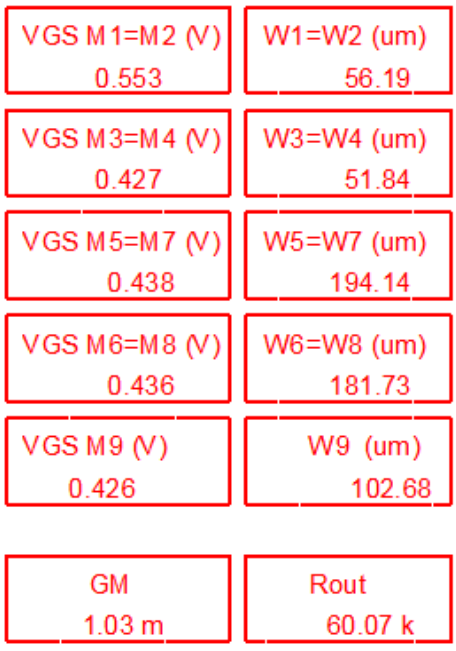



Figure 6-3 Simple OTA Design Parameters, Transconductance and Output Resistance

The use of the slider setup of Figure 6-2 will be used in a series of simple test cases to give the reader insight on how this setup can be used in several scenarios. Let us design an OTA with $V_{DD}+V_{SS}=2V$, L=0.5 um and a differential pair current of 50 µA, it will require a $GM_{OTA} \geq 1.0$ mA/V and $R_{OUT} \geq 25$ kΩ. The simple OTA has been set up in ADS such that the transconductance and output resistance can be measured.

### 6.2.1 Test #1: $V_{GS} \neq V_{DS}$ for Diode Connected transistors.

The design parameters for this case are shown in Figure 6-3, notice that the slider setup is predicting a $GM_{OTA}$ = 1.03 mA/V and $R_{OUT}$=60.07 kΩ. The slider setup was set such that there is DC offset of -400 mV, Kfac=1, IC=1 for the entire OTA, and the diode connected transistors are not meeting the $V_{GS} \neq V_{DS}$ requirement. The results of the simulation are shown in Figure 6-4. Notice that the value of $GM_{OTA}$ has a total error of 12% and $R_{OUT}$ has a 25.6% error from those predicted by our slider setup and shown in Figure 6-3. This large error is produced mainly because the DC current for the output current mirrors is 54.4 µA instead of the 50 µA as per our design. This increase in output current acts like an apparent increase in $K_i$ for equations (6.8) and (6.9) which explains why the transconductance increased and the output resistance decreased.

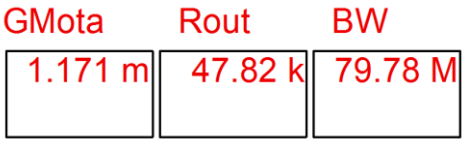



Figure 6-4 Simple OTA $V_{GS} \neq V_{DS}$ for Diode Connected Transistors and DC offset simulation results

### 6.2.2 Test #2: $V_{GS} = V_{DS}$ for Diode Connected transistors (M5 & M7)

The design parameters for this case are shown in Figure 6-5a, notice that the slider setup is predicting a $GM_{OTA}$ = 1.01 mA/V and $R_{OUT}$ = 28.57 kΩ. The slider setup was set such that there is still a DC offset of -400 mV. The IC had to be adjusted because as seen in Figure 6-2 the $V_{GS}$ value of the diode connected transistors do not match their $V_{DS}$ values. In the setup of Figure 6-2 we allow all transistors to have the same IC with the exception of M3 and M4. This arrangement is sufficient to allow us to adjust $V_{GS} = V_{DS}$. In this test case it required that IC=9 for most of the OTA and IC=10 for M3 and M4. However the design resulted in a $GM_{OTA}$=0.459 mA/V which is much smaller than our requirement, the solution is to increase Kfac such that we meet the requirement,

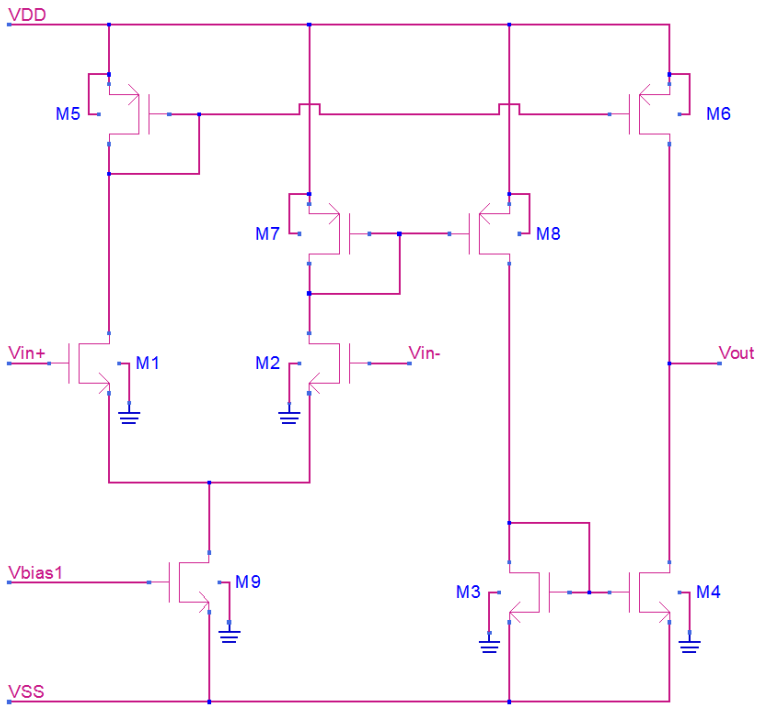
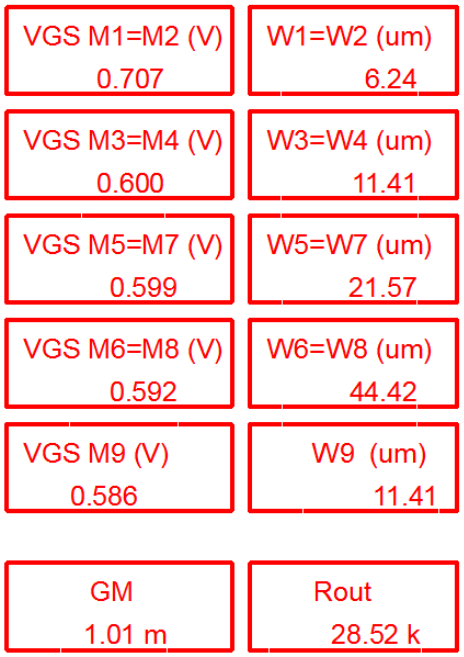
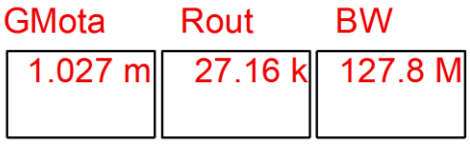



Figure 6-5 Simple Operational Transconductance Amplifier used for all three test cases

Kfac=2.2 gives the $GM_{OTA}$ value shown in Figure 6-5a Setting Kfac-2.2 means that the output current mirrors will have a DC current of $I_D$ = 2.2*50 µA = 110 µA. This change in output current results in a much lower $R_{OUT}$ value but still meets the requirements at28.52 KΩ. The results of the simulation are shown in Figure 6-5b. Notice that the value of $GM_{OTA}$ has a total error of 1.6% and $R_{OUT}$ has a 5% error from those predicted by our slider setup and shown in Figure 6-5a. This error is relatively small compared to the error we got for test case #1 and is acceptable in most applications.




(a)

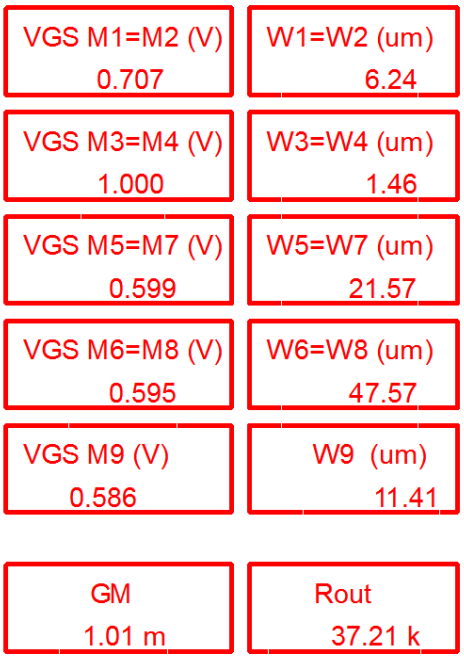



(b)

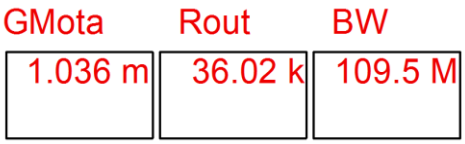
Figure 6-6 Simple OTA $V_{GS}$ = $V_{DS}$ for Diode Connected Transistors and DC offset (a) Design Parameters (b) Simulation Results

### 6.2.3 Test #3: Zero DC offset

In order to get zero DC offset the two output transistors must have the same drain to source voltage, i.e.$V_{DS\_M6}$ = $V_{DS\_M4}$ = 1V. The design parameters for this case are shown in Figure 6-6a, notice that the slider setup is predicting a $GM_{OTA}$ = 1.01 mA/V and $R_{OUT}$ = 37.21 kΩ. The slider setup was set such that there is zero DC offset at the output.




(a)




(b)

Figure 6-7 Simple OTA $V_{GS}$ = $V_{DS}$ for Diode Connected Transistors and Zero DC offset (a) Design Parameters (b) Simulation Results

The zero DC offset was accomplished by setting the sliders such that $V_{DSM4} = V_{DSM6}$. The IC value of M3 had to be adjusted because in order to meet the zero DC offset output requirement we must have $V_{GS\_M3} = V_{DS\_M4}$. In this test case it required that IC=9 for most of the OTA and IC=79 for M3 and M4. However the design resulted in a $GM_{OTA}$=0.439 mA/V which is much smaller than our requirement, the solution is to increase Kfac such that we meet the requirement, Kfac=2.3 gives the GM value shown in Figure 6-5a. Setting Kfac = 2.3 means that the output current mirrors will have a DC current of $I_D$ = 2.2*50 µA = 115 µA. This change in output current results in a much lower $R_{OUT}$ value, when compared to test case #1, but still meets the requirements. The results of the simulation are shown in Figure 6-6b. Notice that the value of $GM_{OTA}$ has a total error of 2.5% and $R_{OUT}$ has a 3.2% error from those predicted by our slider setup and shown in Figure 6-5a. This error is relatively small compared to the error we got for test case #1. It also worth noting that the total DC offset voltage was 2 mV, which is a fantastic result.

The process of designing the simple OTA using the slider setup Figure 6-2 requires the designer to first determine the bias voltage to be used. Voltages are selected such that they meet overall system requirements such as available voltages on the chip or one that can be derived from other sources and the process voltage limits. Current also needs to be determined based on either system level requirements, device current density specifications, power dissipation, etc. The current also has a huge influence in the size of the devices as well. The designer can use some initial guess for inversion coefficient by consulting the MOSFET Operating Plane. For example if large bandwidth is required then moving IC towards strong inversion is the best selection. One can always further

move the sliders for current and IC to get even smaller devices to increase bandwidth further as needed. Usually the $V_{DS}$ voltages are not modified once selected since these changes only provide minor improvements at best. For applications requiring low noise or low voltage then weak inversion is most likely the region to operate in. Incidentally weak inversion is also the region of highest transconductance efficiency so it provides the highest transconductance at the cost of lower bandwidth since the devices are widest in this region. The selection of channel length for the simple OTA is best left for the next section in which three different optimized OTAs are designed and tested. The main variable being used to differentiate among the three types is the channel length. The value of the current gain factor of the output current mirror is used mainly to set the transconductance and output resistance of the OTA. The Kfac value also impacts the bandwidth so we always start with a value of Kfac=1 and then depending on the needed output resistance or bandwidth it can be modified.

## 6.3 Simple OTA Optimized for DC, Balanced and AC Performance

This section explores the same experiments performed by Binkley, et al. in [3] and [7]. The purpose is to design three optimized OTAs, which are AC, balanced and DC optimized, using Binkley's terminology. A DC optimized OTA will operate at lower inversion coefficients and long channel lengths to maximize transconductance and output resistance. An AC optimized OTA operates at high inversion coefficients and short channel lengths to maximize the OTA intrinsic bandwidth. The balanced OTA optimization offers a compromise between DC and AC optimized OTA designs. In section 6.2 we learned that in order to predict the simple OTA performance properly with

the slider setup we need to guarantee that the diode connected transistors obey the $V_{GS} = V_{DS}$ condition otherwise our prediction may be significantly inaccurate. In this experiment we will not require that the DC offset be zero.

The supply $V_{DD}+V_{SS}$ is set at 2V for the three OTA designs. The L values are 0.5 µm, 1.0 µm and 4.0 µm for the AC, balanced and DC OTA designs respectively. The bias current was set at 50 µA. This current value assures that the W values of all transistors are neither exceedingly large that would impact the OTA bandwidth nor too small to where W approaches the value of L. The current gain factor was set to 1 (Kfac=1) as an initial starting point that can be varied later if needed to increase or reduce the overall GM. Using the slider setup of Figure 6-2 the three OTAs were designed and the design parameters are shown in Table 6-1. The inversion coefficient was set for all transistors simultaneously as we did in section 6.2 except for the M3 and M4 transistors so that we could accommodate the diode connected bias requirement. Since the value of $V_{DD}+V_{SS}$ was fixed for all cases at 2V the $V_{DS}$ of transistors M3, M4, M5, and M7 were varied to make sure the diode connected bias

Table 6-1 Simple OTA Optimized Design Parameters

| Device | IC | | | VDS (mV) | | | VGS (mV) | | | W (µm) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DC | Bal | AC | DC | Bal | AC | DC | Bal | AC | DC | Bal | AC |
| M1 - M2 | 3 | 9 | 19 | 700 | 700 | 700 | 574 | 674 | 832 | 150.51 | 12.54 | 3.02 |
| M5 - M7 | 3 | 9 | 19 | 500 | 600 | 700 | 493 | 596 | 698 | 564.26 | 45.34 | 10.07 |
| M6 - M8 | 3 | 9 | 19 | 1500 | 1400 | 1300 | 495 | 592 | 693 | 548.12 | 43.60 | 9.62 |
| M3 - M4 | 6 | 13 | 20 | 500 | 600 | 700 | 493 | 600 | 693 | 67.78 | 7.93 | 2.67 |
| M9 | 3 | 9 | 19 | 800 | 700 | 600 | 436 | 556 | 683 | 267.95 | 22.76 | 5.46 |

condition was satisfied. This requires that the $V_{DS}$ bias voltage for M9, M6 and M8 be adjusted as well to keep $V_{DD}+V_{SS}$ at 2V as seen on Table 6-1.

The three simple OTAs were set up in ADS and simulated with the results shown in Table 6-2. Our results follow closely those tradeoffs obtained by Binkley in that they show that the MOSFET Operating Pane is applicable to the design of CMOS OTA circuits. The circuit with the lowest IC had the highest GM but lowest bandwidth and the one with the highest IC had the highest bandwidth but lowest GM. The reader may notice that in this experiment similar to that in [7] the channel length was changed this is mainly to assure that at the required current of 50 µA each OTA design could reach the desired inversion coefficient. Notice that the DC optimized design has the highest transconductance since it was designed with the lowest IC. The DC optimized design also has the largest output resistance because it was design using the largest L. Consequently the DC optimized simple OTA has the lowest bandwidth since BW is inversely proportional to both L and IC as indicated by the MOS operating plane. The AC optimized design has the lowest GM since it was designed for the highest inversion

Table 6-2 Simple OTA Optimized Design Simulation Results

| | GM (µA/V) | Rout (kΩ) | BW (MHz) |
|---|---|---|---|
| DC | 740.2 | 168.2 | 2.9 |
| Bal | 475.4 | 94.1 | 61.4 |
| AC | 328.1 | 71.5 | 140.9 |

coefficient. The AC optimized simple OTA has the lowest $R_{OUT}$ due to being the design with the lowest channel length. AC optimized simple OTAs will have the highest bandwidth. The balanced simple OTA as expected is a compromise in between the DC

and AC designs. In order to duplicate what Binkley did once one sets L, $V_{DS}$, and I the only value left is IC which is used to set the diode connected conditions.

# 7.0 TECHNICAL SUMMARY AND FUTURE DIRECTIONS

## 7.1 Conclusions

In this thesis our main goal was to develop analog CMOS circuit design methodologies that were both easy to follow and intuitive for the designer. Following a survey of different design methodologies the transconductance efficiency method championed by Binkley et al. was chosen as the basis for our methodologies. The first obstacle that was encountered is that the proposed $g_m/I_D$ methodology was heavily vested in the EKV model which made this kind of method limited in terms of wide spread industry use. In order to get past this limitation a new method to determine $I_0$ using graphical search method was proposed and used effectively.

Once the value of $I_0$ was determined a study of $I_0$ versus $V_{DS}$ and channel length was performed that also included foundry process corners. This thesis confirmed that indeed a single long channel saturated MOSFET can be used to determine the $I_0$ value and that this single value can be used to design CMOS circuit into deep submicron technologies. In this thesis it was also determined that $I_0$ varies with process corners. Despite the $I_0$ variation with process corner it was shown that the transconductance efficiency versus inversion coefficient response is indeed universal for all MOS transistors even in the presence of process variation once the $I_0$ variability is taken into consideration.

Expressions for the gain of the different amplifiers designed in this thesis were developed to take advantage of transconductance efficiency and inversion coefficient techniques proposed by Binkley et al. In order to facilitate the characterization of the MOS transistors needed and to improve on the technique to determine $I_0$ a Y-parameter technique was developed and proven. The Y-parameters technique simplified the determination of $g_m$ and $g_{ds}$. It also provided a means to determine $I_0$ at the same time that these other parameters were being measured, which in turn reduces the number of simulations needed to characterize any process for use with the design methodologies that were developed in this thesis.

Five different types of amplifiers were designed using the methodologies proposed in this thesis. In each design the predicted design specification (e.g. gain, transconductance, etc.) was compared to the results of building the design in the simulator and running the needed simulations. In each occasion it was shown that the difference between our predicted value and the actual circuit was within roundoff error indicating that the design methods actually produced an optimized design for the parameters (e.g. $I_D$, $V_{DS}$, L, etc.). A significant contribution was to show that indeed the MOS operating plane can also be used to guide the design of full CMOS circuits and not just to understand the performance of a single transistor. The performance trends that were done for the amplifier designs performed clearly show that this postulate is valid. Also complete expressions for the gain of the amplifiers studied and for the simple OTA transconductance and output resistance based on the transconductance efficiency ($g_m/I_D$) and current normalized output conductance ($g_{ds}/I_D$) of the MOS transistors were derived. The step by step design methods proved to be both intuitive and easy to follow. Use of

the MOS operating plane is key in determining the need to either increase or decrease different design parameters like channel length, inversion coefficient or bias current, which are the main three design parameters in this method. This design method also includes the drain to source voltage which in many other design methods it is thought to be a secondary parameter but in our method it is included throughout the entire design process.

A proof of concept using the NMOS common source with PMOS current load amplifier design that also determines the gain and output resistance variability was shown. The main idea is to show the designer that as the amplifier is being designed the maximum and minimum performance can be determined. This would allow the designer to make the determination in an early design stage if over process corners the design will work or not. It was interesting to note that a constant $I_0$ value worked well for nominal design as well as corner situations design. There was no need to adjust $I_0$ according to the graphs found. In present industry practice the study of corners impact is a post-design process, i.e. once the design is done the designer must do a series of corner analyses to make sure that the design works at process $\pm 3\sigma$ parameter variations. The unfortunate thing about this latter approach is that if it does not meet the requirements it is back to the beginning and a time costly redesign process which our design method avoids.

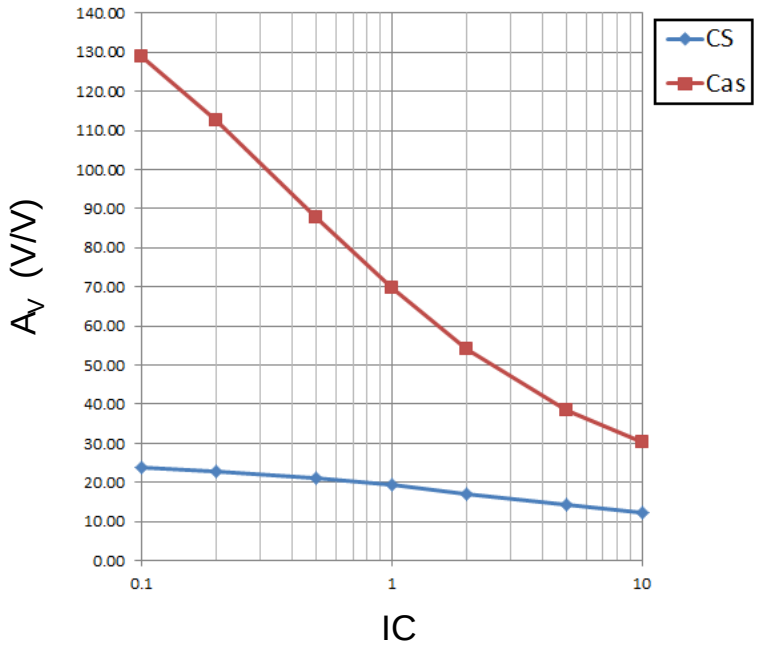
## 7.2 Future Work

As the Common Source with PMOS load amplifier is designed process variability can be analyzed and presented to the designer at the same time. This allows the designer to add this as another design criteria, i.e. how much variation can one expect for the final

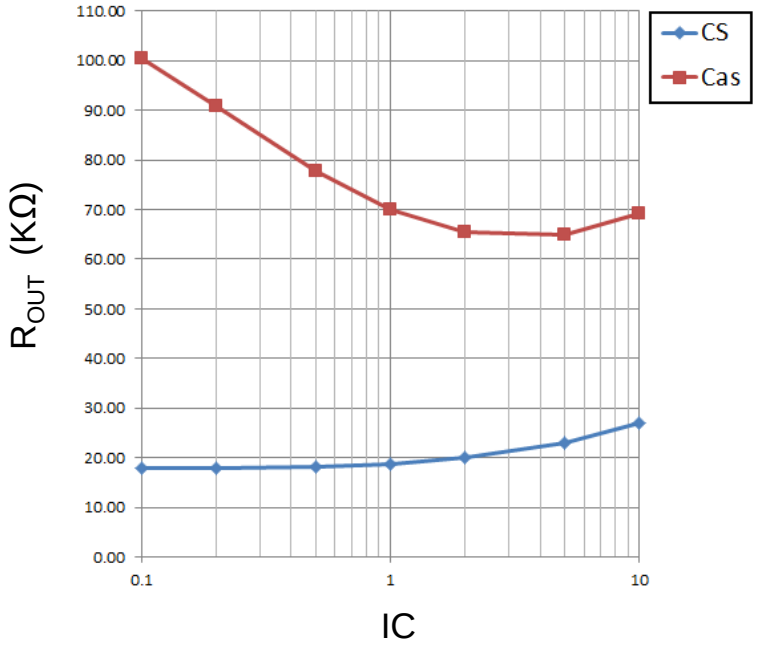
design. The inclusion of process variability for the other configurations studied will be left for future research.

Complete application circuits such as an Operational Amplifiers, Comparators, etc. consists of several stages connected together. Incorporating the requirements on each stage so that the desired performance is obtained when these are connected together to form a complete system is also left for future research. The bias reference voltages and currents needed for each design are assumed to be available in the CMOS technology being used; these circuits can also be designed using similar methods to those used in this thesis. In our design of simple building block circuits we were able very often to assign the same IC values to large groups of transistors in the circuit. This will most likely not be the case when explicit implementation of the bias circuits is included.

During the design process only gain and output resistances performance measures were predicted, some study is needed to include other performance requirements such as bandwidth, non-linearity and noise that perhaps require some further development of the MOS characterization process. For instance, one of the problems that we leave for future study is to investigate whether or not cascoding improves bandwidths of CS and differential amplifiers. It requires a more careful study of the Miller effect and its extent in modern technologies. We have performed some preliminary studies into this topic. The minimum channel length possible for the process was used throughout (L= 0.18 μm) from the tradeoff studies done in chapter 4. The results for these tradeoffs are shown in Figure 7-1. The results shown in Figure 7-1 show the first issue with this analysis, since Miller depends on the gain of the amplifier a logical assessment would be for both ampli-

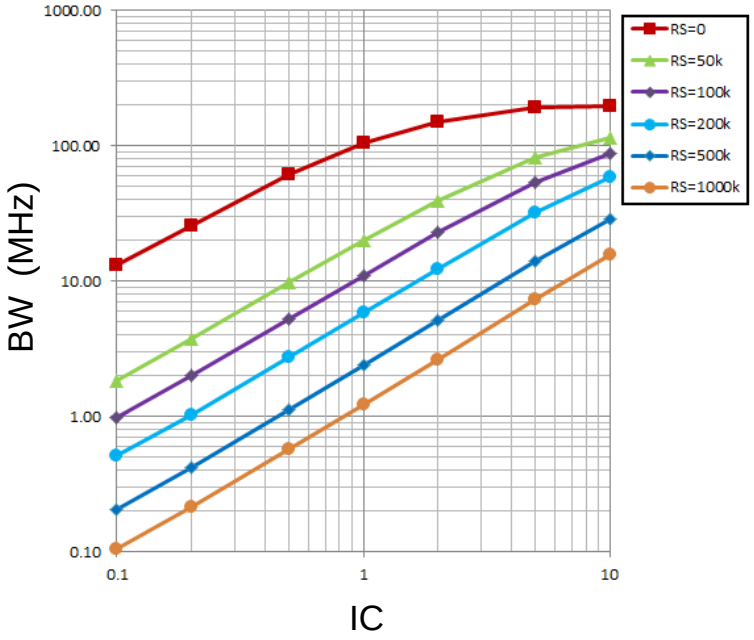



(a)

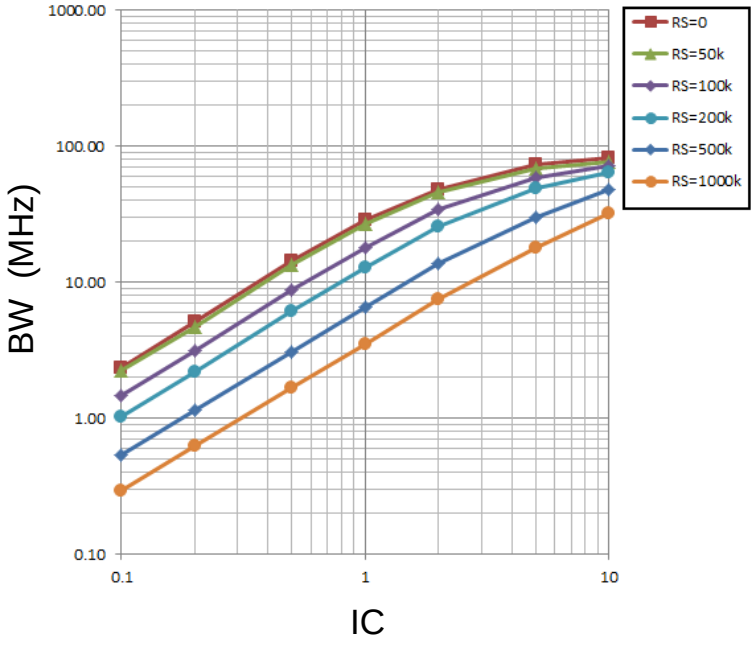



(b)

Figure 7-1: Gain and Output Resistance Tradeoff for L=0.18 µm for (a) Common Source with PMOS Current Load Amplifier (b) Cascode with PMOS Current Load Amplifier




(a)




(b)

Figure 7-2 Bandwidth Tradeoff for L=0.18 µm and Different Values of Source Resistance for (a) Common Source with PMOS Current Load Amplifier (b) Cascode with PMOS Current Load Amplifier

fiers to have the same gain. In chapter 4 we assumed ideal voltage sources driving the amplifiers so the bandwidth was only included by the time constant formed by $R_{out}$ and the output capacitance ($C_{out}$). In order to study Miller's effect several source resistance values were assumed to be driving the amplifier and we measured the simulated bandwidth with the results shown in Figure 7-2. The results indicate that for $R_S$=0 the common source amplifier has the higher bandwidth. However once $R_S$ is a finite value of 50 KΩ the cascode amplifier has better bandwidth but only in the lower values of inversion coefficient (IC < 5). This was unexpected; we were in fact expecting the cascode to have the better bandwidth. The source resistance was then increase to other higher values as shown in Figure 7-2 and we noticed a similar trend for the bandwidth except that the cascode bandwidth has also began to drop again a result we were not expecting. In summary we notice that the cascode bandwidth drops when the source resistance increases and the common source amplifier has comparable bandwidth especially in strong inversion. To further research this topic one needs to deal with the difference in gain and it may be that cascoding to get more bandwidth is no longer a design recommendation.

The stability analysis of the circuits studied (such as the OTA) that may require feedback is also left for future research. In addition stabilization methods for feedback multi-stage op-amps, extending the classical "dominant pole" method is an open problem in the context of model free simulation-based design.

Finally, as our design relied on foundry design kits, it was almost exclusively model free. Here and there several voltage gain and $R_{out}$ formulas had to be justified arguing that small-signal models, similar in structure to ones used in Level 1 modeling,

but of course different in the parameters, can be developed using the EKV model. The compactness of the EKV model allows in principle the development of many theoretical justifications to future graphical analog designs practices that have to rely heavily on simulations, as the designs presented in this dissertation. Binkley's operating plane guidelines were all justified using EKV model formulas. Quite a few analytical design guidelines have been developed by researchers assuming that a complete set of EKV model parameters is available. An interesting future task is to develop model free theoretical design guidelines with the help of the insight coming from the EKV model.

# APPENDIX A: DERIVATION OF THE SQL

In the weak inversion region the $g_m/I_D$ curve is flat; in fact the weak inversion asymptote is a horizontal line that coincides with this flat region as seen in Figure 3-2 [2]. On a logarithmic scale the slope of the strong inversion asymptote is -1/2 for a long device that does not exhibit velocity saturation or VFMR effects. Intersection of the two asymptotes provides the ordinate value of a point that also lies on the strong inversion asymptote line.

Furthermore the maximum transconductance efficiency ($g_m/I_D$) occurs in the weak inversion and it can be expressed as [3]:

$$\left(\frac{g_m}{I_D}\right)_{weak} = \frac{1}{nU_T} \tag{A.1}$$

In strong inversion (without saturation velocity effects) the transconductance efficiency is given by [3]:

$$\left(\frac{g_m}{I_D}\right)_{strong} = \sqrt{\frac{1}{I_D}\left(\frac{\mu C_{ox}}{n}\right)\left(\frac{W}{L}\right)} \tag{A.2}$$

Equation (A.2) shows that in strong inversion the slope of the transconductance efficiency is indeed -1/2 as seen in Figure 3-2 [2].

Based on the definition of the weak inversion asymptote it is a horizontal line that coincides with the maximum transconductance efficiency and intersects the strong inversion asymptote (to be denoted from now on as SQL) precisely at a drain current $I_D = I_0$. The SQL equation is derived from the fact that the slope and a point (where $I_D = I_0$) are known as follows:

$$\log(Y) - \log(Y_A) = m[\log(X) - \log(X_A)]$$

$$\log(Y) = m\left[\log\left(\frac{X}{X_A}\right)\right] + \log(Y_A)$$

$$= \log\left(\frac{X}{X_A}\right)^m + \log(Y_A)$$

$$= \log\left[Y_A\left(\frac{X}{X_A}\right)^m\right]$$

*where*

$$Y_A = \left(\frac{g_m}{I_D}\right)_{weak} = \max\left(\frac{g_m}{I_D}\right)$$

$$Y = \frac{g_m}{I_D}$$

$$X_A = I_o$$

$$X = I_D$$

Therefore strong inversion asymptote line can be expressed in the following form:

$$SQL = \log\left(\max\left(g_m/I_D\right)\left(I_D/I_o\right)^{-1/2}\right) \qquad \text{(A.3)}$$

where $I_D$ is the measured or simulated drain current and $I_0$ is the MOS technology current.

## APPENDIX B: POST-PROCESSING OF MOS CHARACTERIZATION DATA USING ADS

The characterization process discussed in section 4.4 is used for both NMOS and PMOS transistors in different configurations (e.g. common source or common gate). Data from this characterization is then post-processed to obtain the values of IC, $g_m/I_D$ and $g_{ds}/I_D$ required for the design of the several CMOS circuits developed in this thesis. These results are then used to determine the W and $V_{GS}$ design parameters needed for each design. The designer has several choices for the channel length (L), Inversion Coefficient (IC) and drain to sources ($V_{DS}$) of each transistor. In the ADS design setup a series of sliders have been set up so that the user can select these values and the post-processing

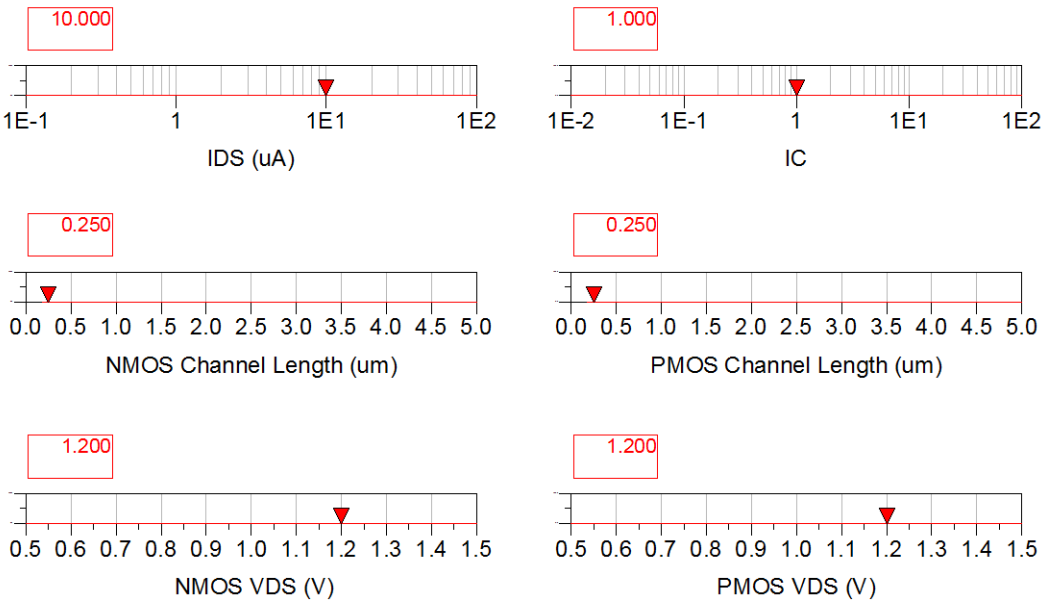



Figure B-1 NMOS CS with PMOS Current Load Amplifier Design – Sliders Setup

capabilities in ADS will then show the designer the performance value (e.g. gain) of the circuit being designed as these sliders are perturbed. This setup can also be done in any other tool as long as the data is made available in a format that is suitable to this third party tool (e.g. Matlab). This can be done since no special ADS feature is needed for the design, making our technique universal. The slider setup is design specific. The one shown in Figure B-1 is for a NMOS common source with PMOS current load amplifier and it is the same as that shown in the body of the thesis as Figure 4-4. It was repeated here for the benefit of the reader.

Post-processing of this data starts with the selections of the values provided by the sliders. The user would determine the value of $I_{DS}$ and $V_{DS}$ based on the overall requirements such as power dissipation and bias voltage (e.g. $V_{DD}$) that are available, etc. Notice that in Figure B-1 there is only one slider for a current labeled "IDS". This is appropriate because in the design of Figure 4-1 both transistors will have the same quiescent drain current. The range of IDS was set as $0.1\mu A \leq IDS \leq 100\ \mu A$ with a $0.1\mu A$ increment and it can be changed by the user as needed. The drain to source voltage of each transistor can in general be different and therefore a slider is provided for each transistor labeled "NMOS VDS" and "PMOS VDS" respectively and the range is taken directly from the characterization results since $V_{DS}$ for each transistor was a swept value in the characterization simulation. Channel length was also taken from the characterization results, the values used are 0.18 µm, 0.25 µm thru 0.75 µm in 0.25 µm steps and 1.0 µm thru 5.0 µm in 1.0 µm steps. In order to modify the range of values for $V_{DS}$ or L the characterization analysis would have to be rerun to include the new values. The values for IC are set by an array variable called "ICval" as shown in Figure B-2. The

ICval array has values 0.01 to 0.1 in 0.01 increments, 0.2 to 1.0 in 0.1 increments, 2 to 9 in increments of 1 and 10 to 100 increments of 5. These values were selected based on our experience and seem to cover the needed range. In an early stage of development we did the entire range from 0.01 to 100 in 0.01 increments that resulted in 10,000 points but this was deemed overkill, just too many points. In ADS all data is saved in arrays. The function of the sliders is to select the value and to also indicate the index location in the array for this value so that we can search the data and pull out other parameters needed that correspond to the design values selected by the sliders. Next we describe how this is done.

```
Eqn ICval=[0.01::0.01::0.1,0.2::0.1::1.0,2::1::9,10::5::100]
Eqn IDspec=Ids*1e-6

Eqn gm_nm=real(Y(2,1)[0]-Y(1,2)[0])
Eqn gds_nm=real(Y(2,2)[0]+Y(1,2)[0])

Eqn IOn=502.6 nA
Eqn ICn=$nmos..ID[lenn,::,0,::]/(100*IOn)

Eqn gm_n=gm_nm[lenn,mn,0,::]
Eqn gm_ID_n=vs(gm_n/$nmos..ID[lenn,mn,0,::],ICn[mn,::])
Eqn gds_n=gds_nm[lenn,mn,0,::]
Eqn gds_ID_n=vs(gds_n/$nmos..ID[lenn,mn,0,::],ICn[mn,::])

Eqn gm_ID_nn=interpolate("linear", gm_ID_n, 1, ICval)
Eqn gds_ID_nn= interpolate("linear", gds_ID_n, 1,ICval)

Eqn VGSn=vs($nmos..DC.VGS[lenn,mn,0,::],ICn[mn,::])
Eqn VGSnn= interpolate("linear", VGSn, 1,ICval)
```

Figure B-2 Post-Process of characterization data using ADS Equations

The discussion below is based on Figure B-2. A slider is provided for the drain current of both transistors and is assumed to be in units of µA. However the slider actually selects just numbers without units to make it visually easy to follow, otherwise ADS would use the exponential notation which we decided to avoid. The variable IDspec takes the value from the IDS slider which is saved in a variable called "Ids" and multiplies it by 1e-6 in order to convert it to units of µA. Variables gm_nm and gds_nm stand for the transconductance and conductance, in this case the _nm stand for NMOS (the PMOS equivalent would have _pm). It is important to indicate that the equations shown in Figure B-2 are for the NMOS and are the same set used for the PMOS. Notice that the values for $g_m$ and $g_{ds}$ are calculated from their Y-parameter definition in section 3-4. The value of the technology current is specified in variable IOn. The inversion coefficient can therefore be calculated using the DC drain current from the characterization simulation. In ADS notation a $ in front of a variable means that we have set up a dataset alias so that it is easy to remember a particular dataset, for the NMOS characterization we use $nmos. Therefore the value of the inversion coefficient is calculated in the variable ICn and thus implements equation (2.1). Note that the drain current in the dataset notation is $nmos..ID and the shape factor used in the characterization is W/L=100.

The next steps are to normalize gm and gds by the drain current and select the values based on the slider selections. Following the equations in Figure B-2 the transconductance for the slider selection is "pulled out" of the array and is set to variable gm_n=gm_nm[lenn,mn,0,::] . Notice that the transconductance gm_nm is dependent on those variables that were swept as part of the characterization of the transistor, namely

channel length, VDS and VGS. In our case it will also include an index that is due to the optimization used to determine I0. The index "lenn" comes from the NMOs channel length slider, mn comes from the VDS NMOS slider and the zero is used to eliminate the I0 optimization dependency. The "::" character is a wildcard selection in ADS so that we have not eliminated the dependency on VGS so far. Actually the Inversion Coefficient expression now deserves some further explanation as well. Note that ICn=$nmos..ID[lenn,::,0,::]/(100*IOn), therefore ICn has been selected for a specific channel length. This allows us to use ICn values vs. VDS and VGS as needed. We now get to the transconductance efficiency:

gm_ID_n=vs(gm_n/$nmos..ID[lenn,mn,0,::],ICn[mn,::]).

Notice how we divide gm_n by the drain current, i.e. gm_n/$nmos..ID[lenn,mn,0,::]. Our interest is in creating our $g_m\_I_D$ and $g_{ds}\_I_D$ versus inversion coefficient and for this reason we use the vs() function in ADS. In the gm_ID_n variable we select ICn for the NMOS VDS voltage selected from the slider and then the vs() function creates an array of $g_m\_I_D$ vs. IC. The determination of $g_{ds}\_I_D$ vs. IC is done in a similar fashion using variables gds_n and gds_ID_n. We also need to know the $V_{GS}$ vs. IC relationship and that is determined via variable VGSn.

The values of ICn come from the characterization process that is a fine sweep of $V_{GS}$ because we do not want to limit ourselves in terms of any value of IC that may be needed. However the IC slider has a finite set of values specified by ICval. A set of new variables was then created that contain only the values of each parameter vs. IC but only to include the values in ICval. These new variables are VGSnn, gm_ID_nn and gds_ID_nn. The values in the ICval array are used to indicate to the interpolate() function

at which specific values the corresponding value is needed, this is necessary so that when the user moves the slider IC the correct value for $g_m\_I_D$, $g_{ds}\_I_D$, and $V_{GS}$ are selected from the data that correspond to the selected IC.

Our post-processing approach has so far reduced the three main parameters needed to be only IC dependent because all other dependencies have been selected already. The IC slider points to an index variable named "idx" which we can use in the three main variables to determine any specification such as voltage gain. In the NMOS Common Source with PMOS Current Source Load Amplifier design we can now implement equation (4.4). The implementation of (4.4) is done in ADS using variable Avi shown in Figure B-3. Notice that Avi is the gain vs. IC since all the variables used in this equation have the same IC dependency. In order to determine the gain at the IC selected by the slider we use the idx index, i.e. Avi[idx]. The same is done when we want to know

```
Eqn SFn=IDspec/(ICval[idx]*IOn)
Eqn Lspecn=$nmos..DC.len[lenn]
Eqn Wdesn=SFn*Lspecn

Eqn SFp=IDspec/(ICval[idx]*IOp)
Eqn Lspecp=$pmos..DC.len[lenp]
Eqn Wdesp=SFp*Lspecp

Eqn Avi=gm_ID_nn/(gds_ID_nn+gds_ID_pp)
```

Figure B-3 Gain and Transistor Width Calculations in ADS

the $V_{GS}$ that corresponds to the IC selected, i.e. VGSnn[idx]. By equation (2.1) the value of W can be determined. The shape factor is determined first using the equation for SFn as shown in Figure B-3. The actual channel length comes from the L slider and is

contained in the variable Lspecn. Once the shape factor and the length are known the determination of W becomes rather trivial and is done with the equation for Wdesn. In Figure B-3 we also show the ADS equations needed to determine the W of the PMOS transistor which is done in the same way as we did for the NMOS.

## APPENDIX C: DETERMINATION OF MOS THRESHOLD VOLTAGE

Our main reference on how to determine the MOS threshold voltage ($V_{TH}$) is [11]. In [37, 38] the interested reader will find further discussion and more advanced techniques of how to extract $V_{TH}$. We show how the technique of [11] is implemented in ADS using a TowerJazz CA18HB design kit MOS device. The basic Level 1 model drain current equation for a saturated MOS is:

$$I_D = K'\left(\frac{W}{2L}\right)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{C.1}$$

It is first assumed that $\lambda$ is small enough so that for all possible values of $V_{DS}$ the $\lambda V_{DS}$ term of equation (C.1) is negligible compared to 1. Under this assumption (C.1) simplifies to:

$$I_D = K'\left(\frac{W}{2L}\right)(V_{GS} - V_{TH})^2 \tag{C.2}$$

(C.2) can be manipulated algebraically as follows:

$$I_D^{1/2} = \left(\frac{K'W}{2L}\right)^{1/2} V_{GS} - \left(\frac{K'W}{2L}\right)^{1/2} V_{TH} \tag{C.3}$$

which is a straight line equation:

$$y = mx + b \tag{C.4}$$

(C.3) is therefore recognized as a straight line having a slope m and a y intercept b. Comparing (C.3) with (C.4) yields:

$$y = I_D^{1/2} \tag{C.5}$$

$$x = V_{GS} \tag{C.6}$$

$$m = \left( \frac{K'W}{2L} \right)^{1/2} \tag{C.7}$$

$$b = -\left( \frac{K'W}{2L} \right)^{1/2} V_{TH} \tag{C.8}$$

Therefore when plotting equation (C.3) (see Figure C-1) we obtain a straight line where the slope is determined by (C.7) and assuming that we know the aspect ratio of the transistor we can determine K'. In a subsequent step the value of the y intercept and the value of K' using equation C.8 yields $V_{TH}$.

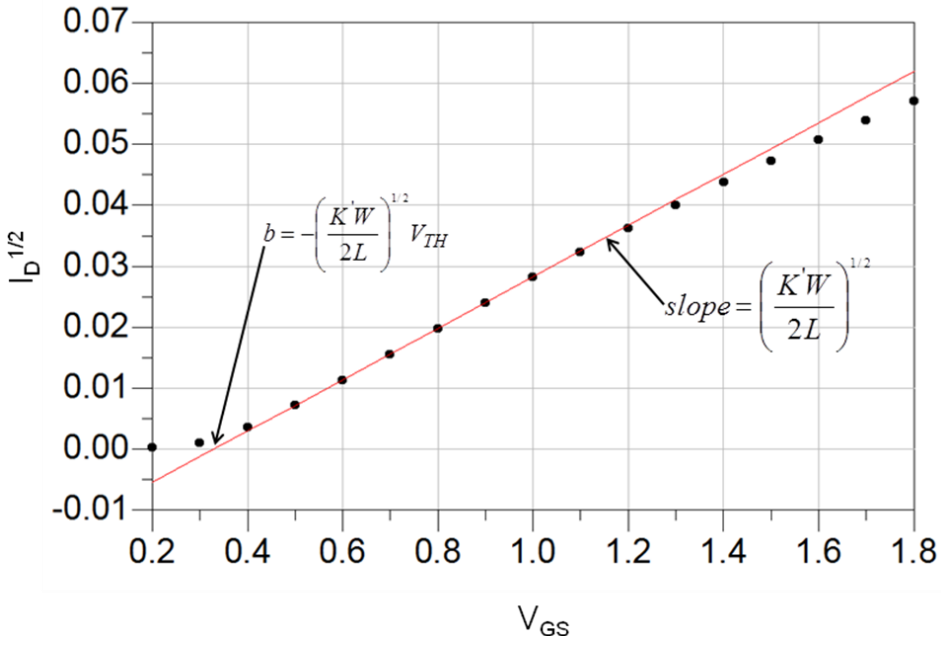



Figure C-1 $I_D^{1/2}$ vs. $V_{GS}$ for a TowerJazz NMOS W/L=16 and L= 2µm

Numerical techniques such as linear regression can be used to extract these parameters instead of graphical technique such as the one shown in Figure C-1. In

choosing a device to determine $V_{TH}$ it is very important that W and L be chosen large enough such that the effective width and length is as close as possible to the drawn values [11]. This will guarantee accuracy whenever extracting K' and $V_{TH}$. The data points in Figure C-1 were obtained for a TowerJazz NMOS device by setting $V_{DS}$=1.0 V and sweep $V_{GS}$ with W/L = 16 and L= 2µm. Second order effects such as sub-threshold conduction at $V_{GS} \leq V_{TH}$ or mobility degradation at high values of $V_{GS}$ can result in a best fit line that is perturbed and therefore results in incorrect values of K' and $V_{TH}$.

Using the data for the NMOS transistor from Figure C-1, that is shown in Table C-1 and linear regression formulas based on equation (C.4), we can determine the slope and the y intercept point as follows:

$$m = \frac{\sum x_i y_i - \left(\sum x_i \sum y_i\right)/N}{\sum x_i^2 - \left(\sum x_i\right)^2 / N} \tag{C.9}$$

$$b = \bar{y} = m\bar{x} \tag{C.10}$$

Table C-1 $I_D^{1/2}$ vs. $V_{GS}$ Data Points

| VGS | sqrt(IDS.i) | slope |
|---|---|---|
| 0.2000 | 0.0003 | 0.0087 |
| 0.3000 | 0.0011 | 0.0254 |
| 0.4000 | 0.0037 | 0.0366 |
| 0.5000 | 0.0073 | 0.0404 |
| 0.6000 | 0.0114 | 0.0420 |
| 0.7000 | 0.0156 | 0.0425 |
| 0.8000 | 0.0198 | 0.0423 |
| 0.9000 | 0.0241 | 0.0417 |
| 1.0000 | 0.0282 | 0.0407 |
| 1.1000 | 0.0323 | 0.0396 |
| 1.2000 | 0.0363 | 0.0383 |
| 1.3000 | 0.0401 | 0.0369 |
| 1.4000 | 0.0438 | 0.0355 |
| 1.5000 | 0.0473 | 0.0340 |
| 1.6000 | 0.0507 | 0.0325 |
| 1.7000 | 0.0540 | 0.0311 |
| 1.8000 | 0.0571 | |

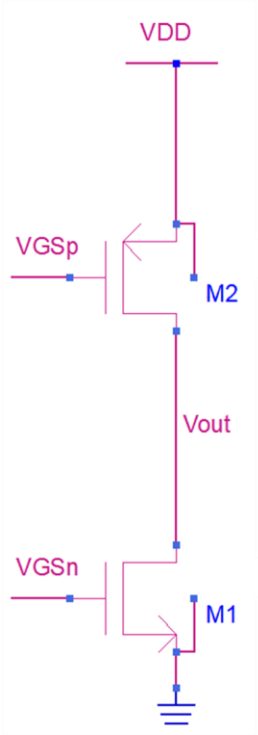
The data must be checked for linearity before linear regression can be applied. We check for linearity by calculating the slope between data points using the following formula:

$$slope = \frac{\sqrt{I_{D2}} - \sqrt{I_{D1}}}{V_{GS2} - V_{GS1}} \tag{C.11}$$

The results for slope are shown in Table C-2. The values outside the rectangle are either too close to subthreshold conduction or affected by mobility degradation on the high side and are not used in the linear regression. Therefore we only use the points that are inside the indicated rectangle for the determination of K' and $V_{TH}$. After evaluation of equation (C.9) and (C.10) we obtain that K'=223.5 uA/$V^2$ and $V_{TH}$= 0.331 V.

# APPENDIX D: DISCUSSION OF COMMON DESIGN PRACTICES AND OPTIMIZATION METHODS AND WHAT CAN GO WRONG

Let us discuss a few hypothetical scenarios that illustrate different possible approaches used in industry for analog CMOS design. In our first scenario let us assume that the designer has inherited the design shown in Figure D-1 from a prior product design and is asked to implement the same design in a newer technology using a simulator equipped with an optimizer. The initial design was done in a 2.0 µm process and the specification is to move to a 0.5 µm process and still meet the same gain requirement but with the smaller channel length and consequently higher bandwidth. Let us assume that the original gain requirement was $|A_v| \geq 100$ and the required bandwidth was BW ≥ 5 MHz. However if BW were greater than 25 MHz then it is assumed that this could open further opportunities to sell the product for new applications. The designer's task is to move the design to the 0.5 µm process with $|A_v| \geq 100$ and BW ≥ 25 MHz without any increase in the circuit power consumption, i.e. while keeping the drain current $I_D$ and the $V_{DD}$ supply the same. In this hypothetical example an alert reader may notice that $V_{DD}$ has not been scaled down along with the transistor channel length reduction as may be required by the technology. The reason that it is done here is to emulate what some inexperienced designers might do while still obeying the foundry process specification (that in our case was provided by Towerjazz [14, 15]).




| | |
|---|---|
| ID | 100 uA |
| VDD | 3.0 V |
| Ln | 2.0 µm |
| Lp | 2.0 µm |
| Wn | 40 µm |
| Wp | 162 µm |
| VGSn | 548 mV |
| VGSp | 605 mV |

Figure D-1 Common Source with Current Load Amplifier Design for L=2.0 µm

Note: In this dissertation all PMOS voltages (e.g. $V_{GS}$ and $V_{DS}$) are shown as positive however PMOS transistors require that these are implemented as negative voltages. Whenever the circuits are implemented the aforementioned voltages are indeed negative throughout the entire dissertation.

A practical first step is to benchmark the design of Figure D-1 in the 2.0 µm process to observe how well it is meeting the requirements. If the requirements are met then one could try converting the circuit to the new technology of 0.5 um by scaling the dimensions by a factor of 4 each in order to keep the W/L or aspect ratio the same and see if any fine tuning or tweaking is necessary to complete the design. After building the circuit in ADS and running AC and DC analyses the results are as shown in Figure D-2.

The results show that the original design has a gain $A_V$ = 104.1 V/V and

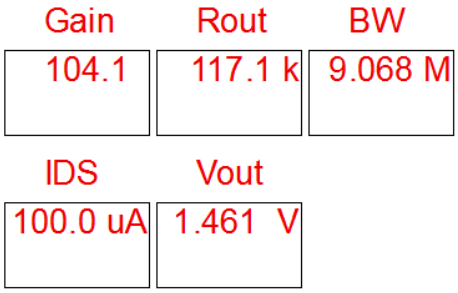



Figure D-2 Common Source with PMOS Load 2.0 µm Design Simulation Results

a bandwidth BW = 9.068 MHz. The designer presumably thereafter decides to scale the design by a factor of 4 making $L_N = L_P$ = 0.5 µm, $W_N$ = 10 µm, $W_P$ = 40.5 µm and the analyses are performed again with the results shown in Figure D-3. The results show that the scaled design has a gain $A_V$ = 5.35 V/V and a bandwidth BW = 317.7 MHz. The gain of this design is nowhere near the requirements while the bandwidth is being met with

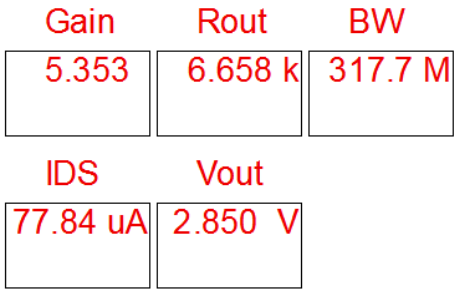



Figure D-3 Common Source with PMOS Load 0.5 µm Initial Scaled Down Design Simulation Results

lots of margin. The fact that the BW is being met with so much margin is encouraging at this point. Observing the bias results the designer realizes that the bias has changed significantly with the new drain current being $I_D$ = 77.84 µA and likewise a change in

$V_{OUT} = V_{DS1} = 2.85V$ from a desired $I_D = 100\ \mu A$ and $V_{DS1} = 1.5V$. This change in the bias is due to some of the small geometry effects like channel length modulation, threshold voltage length dependencies, possible velocity saturation, etc.

A possible solution to bring the design back into compliance is to modify the gate to source voltages ($V_{GS}$) for both transistors. The designer has available ADS with its powerful optimizer hence a decision to make $V_{GSN}$ and $V_{GSP}$ optimizable variables with the DC and gain requirements as the optimization specifications. Once the optimization is complete $V_{GSN} = 579$ mV and $V_{GSP} = 583$ mV which at a first look seems a reasonable change when compared to the values shown in Figure D-1 for the original design. However the optimizer has not been totally successful, "complaining" that "a local minimum has been found". Despite the optimizer not completing the task the designer decides to run the simulation with the newly found gate to source voltages for the scaled down design, the results are shown in Figure D-4. Not surprisingly the results show that

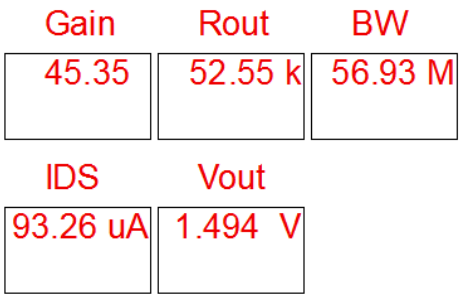
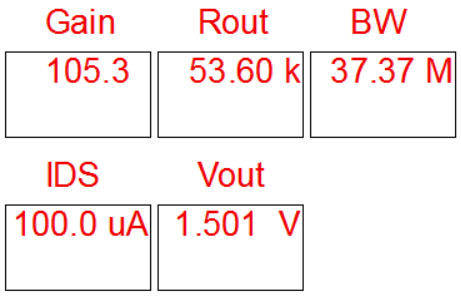



Figure D-4 Failed Optimizer Design Simulation Results

the gain is $A_V = 45.35$ V/V which still does not meet the requirements and the bias current $I_D = 93.26\ \mu A$ is still slightly off. This is the first of several pitfalls in this approach; the designer did not recognize that there are three specifications, i.e. drain

current, drain to source voltage and gain. However there are only two design degrees of freedom in the optimizer, in other words there are not enough degrees of freedom for the optimizer to succeed.

The designer then presumably decides to add more optimizable variables to increase the degrees of freedom for the optimizer. Transistor width for both NMOS and PMOS are then made optimizable and the optimization is run again. The optimization was successful as seen in Figure D-5. However the aspect ratios are nowhere near the values of the original design and the gate to source voltages have also changed




| | |
|---|---|
| ID | 100 uA |
| VDD | 3.0 V |
| Ln | 0.5 µm |
| Lp | 0.5 µm |
| Wn | 78.5 µm |
| Wp | 8.0 µm |
| VGSn | 433 mV |
| VGSp | 867 mV |

Figure D-5 Optimized with 4 Degrees of Freedom Results

significantly when compared to the original 2.0 micron design. Other scenarios are possible, e.g., the optimizable variables were set to be the gate to source voltages and the width of the NMOS transistor, the PMOS width was set fixed at 40.5µm. This latest scenario resulted in a design in which $W_N$ = 132 µm, $V_{GSN}$ = 409 mV, and $V_{GSP}$ = -591 mV with a gain $A_V$ = 105 V/V and a BW = 25.1 MHz. This second optimized design is not as good as the first one because the BW requirement is just being met marginally.

These scenarios indicate clearly some of the pitfalls related to this optimization-based approach. Notice that the problem is that the designer has no way to know clearly how a change in W and $V_{GS}$ will affect the performance of the circuit.

There can be even worse pitfalls for the "blind" optimization approach. In yet another scenario the designer is now presumably asked to design the same amplifier in a 0.18 µm process. Having learned that several possible combinations of W and $V_{GS}$ optimizations will result in different designs, the designer tries several of them and settles on the one that adjusts both widths and both gate to source voltages. Unfortunately no matter what optimizable variables are used the gain specification can never be met and the optimizer runs into a local minimum error as that shown in Figure D-6. The optimization status window of Figure 1-6 shows some very interesting results. Before the optimization stopped it was trying to make W1 (NMOS width) as high as possible (max was set at 500 µm) and at the same time W2 as small as possible (min was set at 0.5 µm).

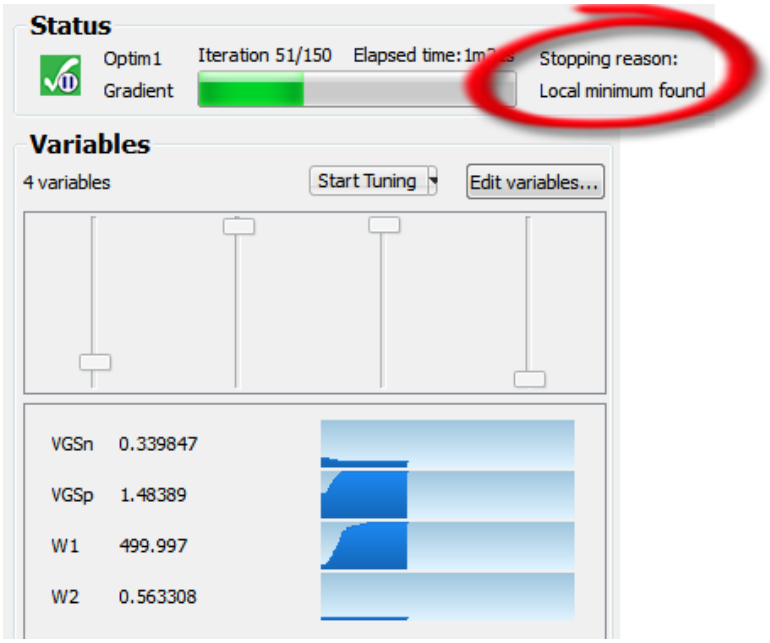



Figure D-6 Optimization status for L=0.18 µm case

Also notice that the values of the gate to source voltages were going to extreme values as well. The issue with this design at 0.18 µm is that this particular amplifier design cannot meet the gain requirement of $|A_V|$ = 100 V/V. Later in this thesis we discuss the concept of Inversion Coefficient and Transconductance Efficiency after which this will become clear. For now let us show the gain of this amplifier for L = 0.18 µm in Figure D-7. The intrinsic gain is that of the NMOS transistor amplifier without any load, this would be the ideal gain with an infinite load and by process limitations it cannot be any higher than approximately 31 V/V. Once the PMOS load is added the maximum gain is reduced to

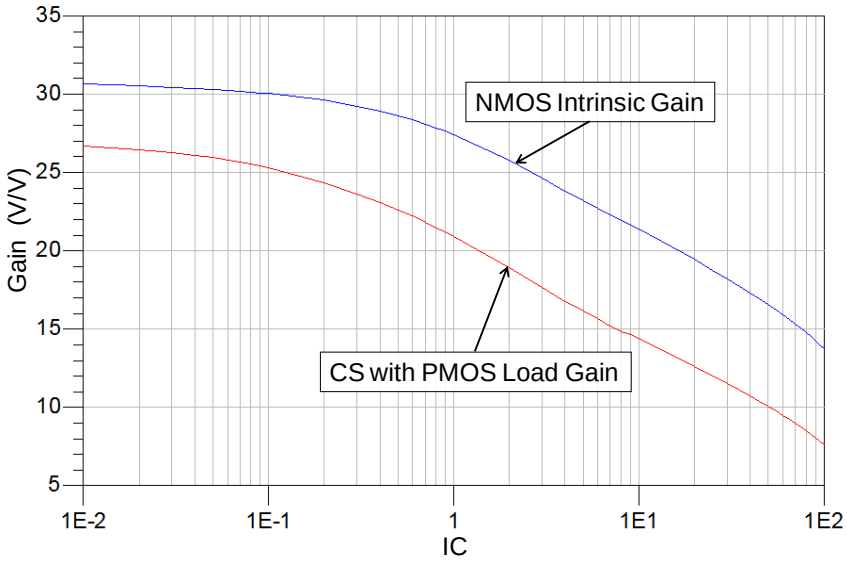



Figure D-7 NMOS Common Source Amplifier Gain

approximately 27 V/V. In a blind optimization approach or any manual formula approach if the designer is not aware of these limitations many hours are spent redesigning and testing the design without the realization that a different topology is needed because the gain requirement just cannot be met using this amplifier topology.

REFERENCES


[1] E. A. Vittoz, “Micropower Techniques,” in Design of MOS VLSI Circuits for Telecommunications, J. Franca and Y. Tsividis, Eds. Englewood Cliffs, NJ: Prentice-Hall, 1994.

[2] Foty, D., Bucher, M., Binkley, D., “Re-interpreting the MOS transistor via the inversion coefficient and the continuum of gms/Id”, Circuits and Systems, 2002. 9th International Conference on Electronics, vol. 3, pp. 1179-1182, 2002.

[3] D. M. Binkley, , C. E. Hopper, S. D. Tucker, B. C. Moss, J. M. Rochelle, and D. P. Foty, “A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 22, pp. 225-237, Feb. 2003.

[4] D. Binkley, B. Blalock, J. Rochelle, “Optimizing Drain Current, Inversion Level, and Channel Length in Analog CMOS Design”, Journal - Analog Integrated Circuits and Signal Processing, vol. 47, issue 2, pp. 137 – 163, May 2006.

[5] F. Silveira, D. Flandre, P. G. A. Jespers, “A gm/ID Based Methodology for the Design of CMOS Analog Circuits and Application to the Synthesis of a Silicon-on-Insulator Micropower OTA”, IEEE Journal of Solid-State Circuits, vol. 31, no. 9, pp. 1314-1319, September 1996.

[6] D. Foty, “Mosfet Modeling with SPICE Principles and Practice”, Prentice Hall, 1997.

[7] D. M. Binkley, “Tradeoff and Optimization in Analog CMOS Design”, Wiley, 2008.

[8] Bucher, M.; Diles, G.; Makris, N., “Analog performance of advanced CMOS in weak, moderate, and strong inversion “, Mixed Design of Integrated Circuits and Systems (MIXDES), 2010 Proceedings of the 17th International Conference, Page(s): 54 – 57, 2010.

[9] B. Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill, New York, 2001.

[10] P. R. Gray, P.J. Hurst, S.H. Lewis, R.G. Meyer, “Analysis and Design of Analog Integrated Circuits”, John Wiley & Sons, 2001.

[11] P.E. Allen, D.R. Holberg, “CMOS Analog Circuit Design”, Oxford, 2012.

[12] Y. Tsividis, C. McAndrew, “Operation and Modeling of the MOS Transistor”, Oxford, 2011.

[13] Advance Design System 2009 Update 1 software manual, Agilent Technologies, Inc., 2009.

[14] Jazz Semiconductor, “Electrical Parameters of the CA18 and CR18 Processes” TowerJazz, Inc. 2009.

[15] Jazz Semiconductor, “Design Application Note for CA18HP, CA18HB, CA18QB, CA18QG, CA18QH, CA18QJ, CA18QE, CA18ME, CA18QK, CA18MK and CA18HA Processes” TowerJazz, Inc. 2011.

[16] Comer, D.J.; Comer, D.T., “Using the weak inversion region to optimize input stage design of CMOS op amps” IEEE Transactions on Circuits and Systems II: Express Briefs, Volume: 51 , Issue: 1 pp., 8 – 14, 2004.

[17] Hollis, T.M.; Comer, D.J.; Comer, D.T., “Optimization of MOS amplifier performance through channel length and inversion level selection”, IEEE Transactions on Circuits and Systems II: Express Briefs, Volume: 52, Issue: 9, pp. 545 – 549, 2005.

[18] S. C. Terry, J. M. Rochelle, D. M. Binkley, B. J. Blalock, D. P. Foty, M. Bucher, “Comparison of a BSIM3V3 and EKV MOST Model for a 0.5um CMOS Process and Implications for Analog Circuit Design”, IEEE Transactions on Nuclear Science, Volume: 50 , Issue: 4 , 2003 , pp. 915 – 920.

[19] Singh, K., Bhattacharyya, A.B., “Transconductance related analysis of EKV MOSFET model for a 0.35 μm CMOS technology node” Mixed Design of Integrated Circuits and Systems (MIXDES), 2010 Proceedings of the 17th International Conference, 2010 , pp. 436 – 440.

[20] Girardi, A., Cortes, F.P., Bampi, S., “A tool for automatic design of analog circuits based on gm/ID methodology”, International Symposium on Circuits and Systems, 2006. ISCAS 2006 Proceedings, pp. 4643-4646.

[21] Maji, S., Dam, S.; Mandal, P., “Automatic generation of saturation constraints and performance expressions for geometric programming based analog circuit sizing” International Symposium on Quality Electronic Design (ISQED), 2011, pp. 1 – 8.

[22] Advanced Analog Integrated Circuit Design Course Reader - EE214 Winter 2011, Boris Murmann, Stanford University.

[23] D. Stefanovic, M. Kayal, “Structure Analog CMOS Design”, Springer 2008.

[24] T. Konishi, K. Inazu, J. G. Lee, M. Natsui, S. Masui, B. Murmann, “Design Optimization of High-Speed and Low-Power Operational Transconductance Amplifier Using gm/ID Lookup Table Methodology” IEICE TRANSACTIONS on Electronics Vol. E94-C No.3 pp.334-345.

[25] R. K. Brayton, G. D. Hachtel, and A. Sangiovanni-Vincentelli, “A survey of optimization techniques for integrated-circuit design,” Proceedings of the IEEE, Vol. 69,No 10, pp. 1334–1362, Oct. 1981.

[26] M. Hershenson, S. Boyd, T. Lee, “Optimal Design of a CMOS Op-amp via Geometric Programming”, IEEE Transactions on Computer-Aided Design, Vol. 20 No.1, pp. 1-21, January 2001.

[27] M. Hershenson, S. Boyd, T. Lee, “CMOS operational amplifier design and optimization via geometric programming” , Proceedings of the First International Workshop on Design of Mixed-mode Integrated Circuits and Applications, Cancun, Mexico, pp.15-18, July 1997.

[28] M. Hershenson, Boyd, and Lee, Automated design of folded-cascode op-amps with sensitivity analysis, 5th IEEE International Conference on Electronics, Circuits and Systems, Lisbon, pp. 121-124, September 1998.

[29] Virtuoso NeoCircuit Datsheet - http://www.cadence.com/rl/Resources /datasheets/ VirNeoCircuit_ds.pdf.

[30] D. F. Wong, H. W. Leong, C. L. Liu, “Simulated Annealing for VLSI Design”, Kluwer 1988.

[31] C. Xinghao and M. L. Bushnell, “Efficient Branch and Bound Search with Application to Computer-Aided Design”, Kluwer, 1996.

[32] D. Bertimas, J. Tsitsikis, “Simulated Annealing”, Statistical Science, Vol. 8 No. 1, pp. 10 – 15, 1993.

[33] C. Enz, F. Krummenacher, E. A. Vittoz, “An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications”, Analog Integrated Circuits and Signal processing, vol. 8, pp 83 – 114, July 1995.

[34] Kurokawa, K., "Power Waves and the Scattering Matrix", IEEE Trans. Micr. Theory & Tech., Mar. 1965, pp. 194-202.

[35] Guillermo Gonzalez, "Microwave Transistor Amplifiers, Analysis and Design, 2nd. Ed.", Prentice Hall.

[36] David M. Pozar, "Microwave Engineering", Third Edition, John Wiley & Sons Inc.

[37] A. Ortiz-Conde, F. J. Garcıa Sanchez, J. J. Liou, A. Cerdeira, M. Estrada,Y. Yue, "A review of recent MOSFET threshold voltage extraction methods", Micro-electronics Reliability Journal, Vol. 42, 2002, pp. 583–596.

[38] Osmar Franca Siebel, Marcio Cherem Schneider, Carlos Galup-Montoro, "MOSFET threshold voltage: Definition, extraction, and some applications", Micro-electronics Journal, Vol. 43, 2012, pp. 329–336.