Canadian Journal on Electrical and Electronics Engineering Vol. 4, No. 2, April 2013

Determination and Study of MOSFET Technology Current

Wilfredo Rivas-Torres, and Zvi S. Roth

Abstract —*CMOS Technology Dependent Current (I_0) is a transistor parameter needed to define the inversion coefficient of the transistor. Designers using the g_m/I_D design methodology may determine I_0 directly from the EKV model parameters. The paper proposes a simple algorithm for finding I_0 from semiconductor foundries that support any MOSFET models, such as BSIM3 and PSP. Through the repeated use of this method the paper resolves several fundamental questions related to the use of the technology current in CMOS analog design. It is shown that I_0 is bias and process dependent. The paper studies the dependence of I_0 on V_{DS} and L. The impact of process corners on I_0 tolerances and on the design performance is also studied. It is demonstrated that such tolerance effects may be significant even in a simple amplifier circuit. Yet it is shown that the assumption of a constant I_0 that significantly simplifies submicron CMOS analog design has no adverse impact on the accuracy of the design. The paper also shows that the transconductance efficiency vs. inversion coefficient MOSFET curve is not affected by process corners thus providing an additional substantiation to the claimed universality of such MOSFET curves. The paper results pave the way to the use of Binkley's Operating Plain design method for transistor models that are other than the EKV model.*[1]

Key Words — CMOS, Inversion Coefficient, MOSFET transconductance efficiency, Sub-micron analog design.

I. INTRODUCTION

A key design parameter in analog CMOS design done in submicron CMOS technology is the MOSFET inversion coefficient IC (aka Inversion Factor). A design methodology that is based on the universal shape of the transconductance efficiency (g_m/I_D) vs. IC curve was developed in [1, 2]. IC is I_D, the DC drain current of the MOS device, normalized by the shape factor W/L (also known as the MOSFET aspect ratio) and a fixed process technology current I_0 [6].

$$IC = \frac{I_D}{I_0\left(\frac{W}{L}\right)} \tag{1}$$

[1] W. Rivas-Torres is with the Computer & Electrical Engineering and Computer Science Department, Florida Atlantic University, Boca Raton, Florida, 33431 USA (tel.: 321-235-2014; e-mail: wrivast@fau.edu).

Z. S. Roth is with the Computer & Electrical Engineering and Computer Science Department, Florida Atlantic University, Boca Raton, Florida, 33431 USA.

For a unity aspect ratio I_0 equals the DC drain current at what is known as the "center of the MOSFET moderate inversion region" [2] where IC = 1. Such a center is first defined by intersecting two well understood behaviors of the graph of g_m/I_D vs. I_D, one that is constant for the weak inversion region and the other that obeys a square law for strong inversion. The latter is taken under the assumption of a long channel. In [3] that intersection solution is:

$$I_0' = 2n\mu C_{OX} U_T^2 \tag{2}$$

where μ is the surface carrier mobility, n is the voltage division ratio between the gate oxide capacitor and the substrate depletion MOS capacitor, C_{OX} is the gate oxide capacitance per unit area, and U_T=kT/q is the thermal voltage. Note that I_0' is not constant, as both n and μ are bias-dependent and technology-dependent. The value of n can be determined from the slope factor n that is a function of the gate voltage [11]:

$$n(V_G) = \frac{1}{1 - \frac{\gamma}{2\sqrt{V_G - V_{TH} + \left(\frac{\gamma}{2} + \sqrt{\psi_0}\right)^2}}} \tag{3}$$

where ψ_0 is the surface potential, γ is the substrate factor (aka body effect factor) ,and V_{TH} is the threshold voltage. An approximation for n is presented in [6]:

$$n(V_G) \approx 1 + \frac{g_{mb}}{g_m} \tag{4}$$

In [3] a constant technology current I_0 is defined as:

$$I_0 = 2n_0\mu_0 C_{OX} U_T^2 \tag{5}$$

where μ_0 is the surface carrier mobility held fixed at its low-field value and n_0 is the voltage division ratio between the gate oxide capacitor and the substrate depletion MOS capacitor held fixed at its average value in moderate inversion. The value of n_0 is then determined either by evaluating (3) in the middle of the transistor moderate inversion region or by measurements of the bulk transconductance (g_{mb}) and of the transconductance (g_m) in the middle of the moderate inversion

region followed by an evaluation of (4).

The process technology current is in general different for each semiconductor foundry process. Once I_0 becomes known a designer can plot the curve of g_m/I_D vs. IC that characterizes the foundry process.

The g_m/I_D CMOS design methodology is attractive as it allows circuit design over the entire MOS operating region (i.e. from weak through strong inversion) [3, 4]. Other graphic MOSFET measurements such as the Early voltage vs. IC and V_{GS} vs. IC that are very important for analog design can be determined as well. Depending on the circuit design specifications a designer using the MOSFET Operating Plane proposed by Binkley can select the channel length L and IC to intuitively determine the sizing of each transistor [3, 4, 6]. The Operating Plane provides the designer with a qualitative dependence of various performance specifications on the inversion coefficient and channel length design parameters selections. Three OTA designs have been reported in [4] that use the insight gained from the operating plane. The three amplifiers used the same bias current but were optimized for different design requirements, one for maximizing bandwidth, another for minimizing DC mismatch and a third for a balance between bandwidth and DC mismatch.

The literature papers that use this design methodology can be divided into two groups (i) analytical and (ii) experimental. The experimental approach uses device characteristic data generated by a simulator (e.g. SPICE) or a set of measured results [8]. The analytical g_m/I_D design methodology utilizes equations motivated by the EKV MOS model [3,4,6]. In [3] expressions for the MOS technology current and other important design equations useful for analog CMOS design are developed. A design methodology is implemented in a prototype CAD system (using Microsoft Excel) permitting the designer to explore the MOS design space of drain current, inversion level, and channel length while observing a graphical view of MOS performances against selected goals. This allows the designer to optimize the sizing of individual MOSFETs (or related groups of MOSFETs).

In [10] an analytical method based on the inversion factor and g_m/I_D is presented. A set of basic building blocks are combined into a library. The building blocks for complete designs are fundamental circuits designed based on the analytical method using the EKV model. A BSIM3 to EKV model converter is presented to assist in such a design approach. This conversion is needed to utilize the EKV expressions for such parameters as I_0, inversion factor and transconductance effciency. A program called PADS then uses the library of basic blocks to complete a larger scale design.

The g_m/I_D experimental design method [8, 9] is based on a graphical lookup approach. This methodology too optimizes individual transistors based on three fundamental plots that include the transit frequency, intrinsic gain and current density (I_D/W) each as a function of g_m/I_D for several channels lengths. The experimental data is obtained from HSPICE operating point for a test MOS device in which the channel length is swept. In [9] the authors use a lookup table to design a low power OTA.

Unfortunately the EKV model is presently supported by very few semiconductor foundries and it is not considered a standard model by the Compact Model Council (CMC). This undeservedly limited the support by the engineering and scientific community to analog design approaches based on Binkley's Operating Plane methodology. As foundries move toward smaller technologies in deep submicron newer models such as the BSIM4 and PSP are nowadays considered standard. In [3] the possibility of utilizing other models like BSIM3 along with the MOS Operating Plane is mentioned and our paper attempts in part to demonstrate how it is done.

The paper starts out by implementing a simple search algorithm based on an idea proposed by Binkley [3] for a determination of I_0 from simulated or measured data. The method is based on numerical search that determines the point of tangency between the theoretical transconductance efficiency in strong inversion and the actual measured (or simulated) transconductance efficiency. Also in this paper is the presentation of the effects of drain to source voltage (V_{DS}), channel length (L) and process variability on the technology current and consequently the effects of I_0 variations on the analog circuit design.

II. I_0 Determination Method

Given any MOSFET model obtained from a semiconductor foundry, the user can always set the aspect ratio W/L to 1, embed the transistor in a simulation test circuit containing a fixed and large enough DC source for V_{DS} to assure saturation mode and a variable DC source for sweeping V_{GS} to obtain a plot of the transconductance efficiency curve g_m/I_D vs. I_D (see Fig. 2). Using such a graph that is based on actual data points the weak inversion horizontal asymptote can be extrapolated from the region where g_m/I_D approaches the thermal voltage limit. The strong inversion asymptote on the other hand on a logarithmic scale, and under the assumption of no velocity saturation effects, has a slope of -1/2 representing the ideal "square law" region of the transconductance efficiency curve. The -1/2 slope is valid only for a sufficiently long device that does not exhibit velocity saturation or VFMR effects and as long as the MOSFET device is operating in saturation mode. The weak inversion and strong inversion asymptotes intersect at what is defined as the middle of the moderate inversion region (also defined as IC=1) at a drain current I_D that equals exactly I_0. The above was proposed by Binkley et al in [2] and is the basis of the I_0 search algorithm.

The graphical determination of I_0 is done by iteratively intersecting the horizontal weak inversion g_m/I_D line with candidate square-law strong inversion region asymptote lines (that all have a slope of -1/2 and an undetermined location). In Fig. 1 the procedure flowchart for the determination of I_0 is presented. The determination of I_0 starts with a unity aspect ratio device setup such that saturation mode is guaranteed and that no terminal voltage exceeds the foundry process maximum

values. Selecting an initial value of I_0, while not a critical selection for this algorithm to work, could be done based on some a-priori reasonable estimates. For example in our simulation experiments a value of 1 µA was used which places the initial strong inversion candidate line to the right of where the actual solution is expected. The weak inversion asymptote

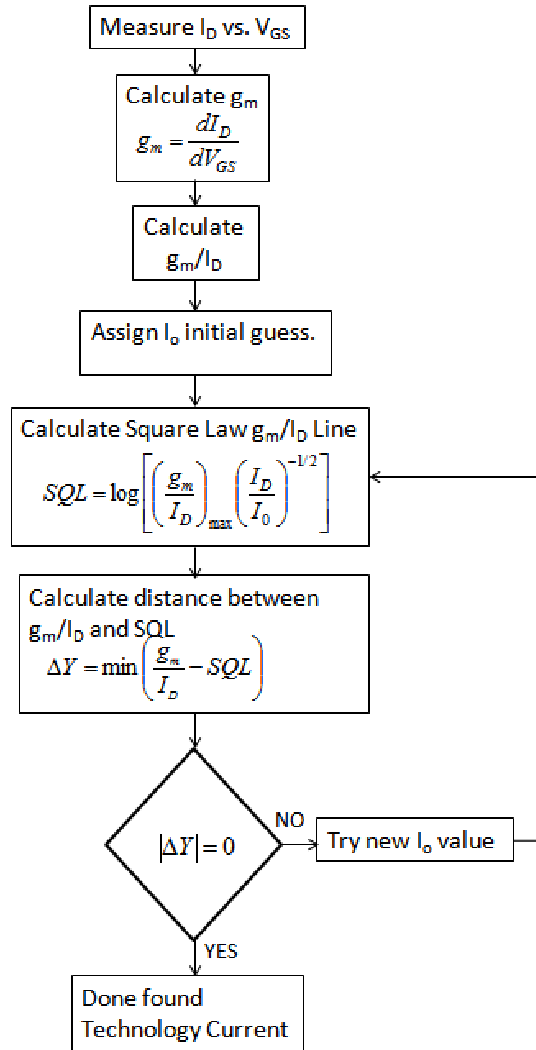

Fig. 1. Technology Current (I_0) Determination Flowchart.

defines a point $[I_0,(g_m/I_D)_{max}]$ on the strong inversion asymptote line. Since the slope and a point are known for the strong inversion asymptote the square law line (SQL) candidate is uniquely defined. The vertical distance between the square law line (SQL) and the g_m/I_D data is then determined by calculating the corresponding vertical value differences for each I_D. The minimum value of these differences is taken as the distance between the two curves. If the distance between the two curves is zero then the SQL line becomes a curvilinear tangent asymptote to the g_m/I_D curve and thus I_0 becomes determined. In [3] the authors indicate that I_0 needs to be determined for a sufficiently long channel. In section IV utilizing this algorithm we show a parametric study that determines how small L must be for an accurate determination of I_0.

III. Measured Transconductance Efficiency vs. Inversion Coefficient

From [3] the value of IC can be calculated using (1). All the parameters needed to plot the transconductance efficiency (g_m/I_D) vs. IC for any MOS device are now available; such a curve is presented in Fig. 3.

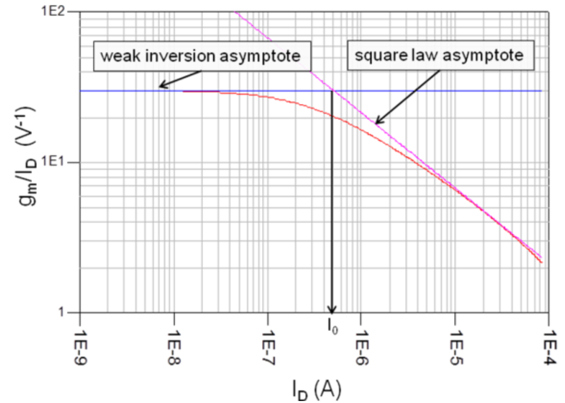

Fig. 2. Transconductance Efficiency g_m/I_D vs. drain current for a TowerJazz NMOS transistor V_{DS}=1.8V. L=4 µm and W/L=1.

ADS (Advance Design System software by Agilent Technologies, Inc.) parameter sweep capabilities can now be exploited in order to study the effect of several parameters (such as channel length) on the transconductance efficiency. The "square law" region of the transconductance efficiency curve is being used to determine the technology current I_0. The results shown in Fig. 4 were obtained using the TowerJazz CA18HB process models and match results similar to those obtained in [3, Fig. 2] and [4, Fig. 2]. The curves of Fig. 4 indicate the universal shape of the g_m/I_D curve can be seen until the effects of velocity saturation become significant (i.e. the slope of the curve drops below the theoretical -1/2) especially for the smaller channel length devices in the strong inversion region of the response.

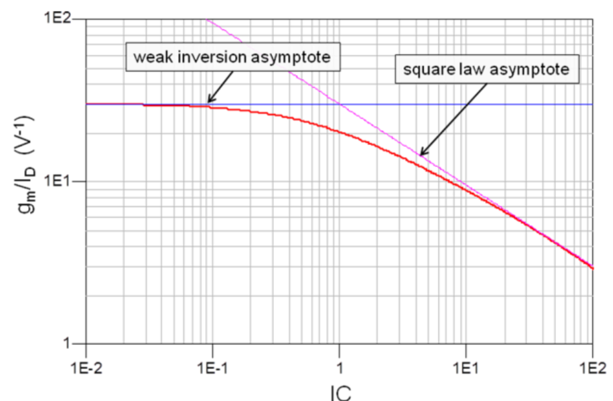

Fig. 3. Transconductance Effciency vs. inversion coefficient (IC) for a TowerJazz CA18HB process NMOS transistor V_{DS}=1.8V, L=4 µm and W/L=1.

IV. Effects of Process Corners, L and V_{DS} on the Identification of I_0

According to Binkley I_0 is intended to be used in analog

design as a constant parameter [3] even though this is only an approximation. Let us start by studying how process dependent I_0 is. Semiconductor foundry MOSFET models typically account for a slow, nominal and fast MOS device. These process corners models depend on several chosen physical parameters like the oxide thickness (t_{ox}), channel doping, drain/source doping, technology (e.g. 0.18 um), reduction in channel length from its drawn value, threshold voltage, etc. The chosen parameters deem to represent the entire process variations. Based on statistical analysis the ±3σ values of each physical parameter are first determined. The 3σ-fast model is found using either the +3σ or the -3σ of each parameter, depending which option yields a larger device current. For instance, for t_{ox} the smaller extreme value is taken as part of the "fast corner" model. Likewise for the 3σ-slow parameters for NMOS and PMOS devices [5, chapter 14]. The search technique developed in section II allows the study of I_0 versus process corners.

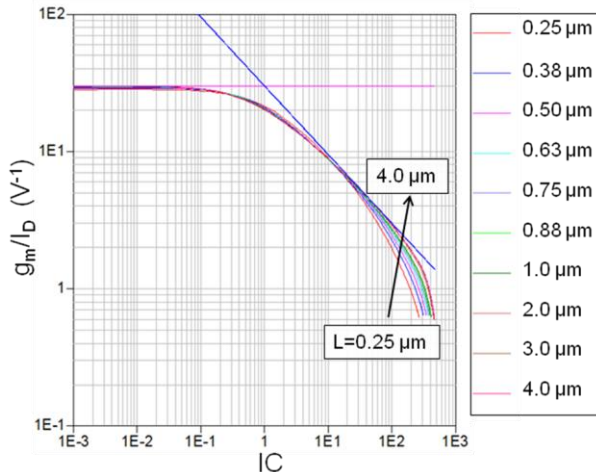

Fig. 4. NMOS Transconductance Effciency vs inversion coeffcient (IC) and channel length (L) for V_{DS}=1.8V and W/L=1.

In order to study whether or not V_{DS} influences I_0 the process of estimating I_0 may be repeated as V_{DS} is swept. The results of this analysis are shown in Fig. 5. A 0.18 µm process NMOS with L = 4 µm and with a shape factor of 1 was used. Note that the value of I_0 drops significantly for V_{DS} < 0.5V. As in saturation I_D is more or less independent of V_{DS}, once the dependency becomes stronger it is an indication of a change of MOSFET conduction mode. In Fig. 5 we notice a change in I_0 dependency on V_{DS} for V_{DS} that approximately equals 0.5V.

The average error for the value of I_0 for V_{DS} > 0.5V is approximately 2% (even for process corners) across the range of bias voltages of practical interest. That is I_0 being a "special current" still obeys basic MOS operation characteristics so it becomes nearly constant for $V_{DS} > V_{Dsat}$. As expected the value of I_0 is fairly insensitive to V_{DS} as long as the MOS device is in saturation. A somewhat surprising observation is that the values of I_0 are quite sensitive to process corners. The I_0 value for a slow process is less than a nominal process with the fast process having the highest value. This can be intuitively deduced from (1) since a faster process has a smaller t_{ox} which in turn means a larger value of C_{ox} and hence a higher value of I_0.

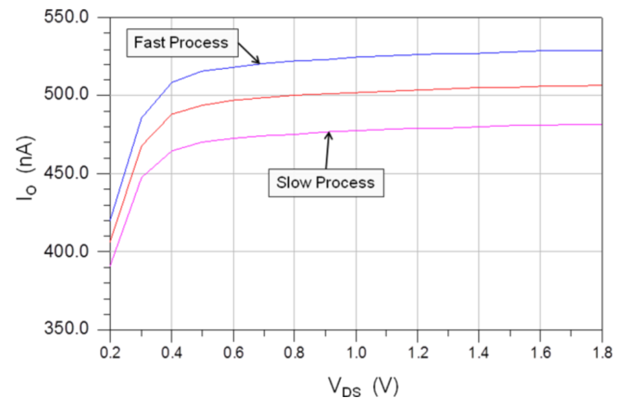

Fig. 5. The identified I_0 vs. V_{DS} and Process Corners for a TowerJazz NMOS L=4 um W/L=1.

From [2] the value of I_0 can be estimated from the intersection of the weak inversion asymptote and the strong inversion asymptotes. It is safe to say that for a "large enough" device one can use this technique to establish a single constant value for I_0 to be used in subsequent sub-micron analog design. Fig. 6 shows technology current estimation results as the channel length for a NMOS device (for V_{DS} = 1.8V) is swept. The results show that using L ≥ 2 µm is a good estimate for the minimum channel length at which I_0 is to be determined.

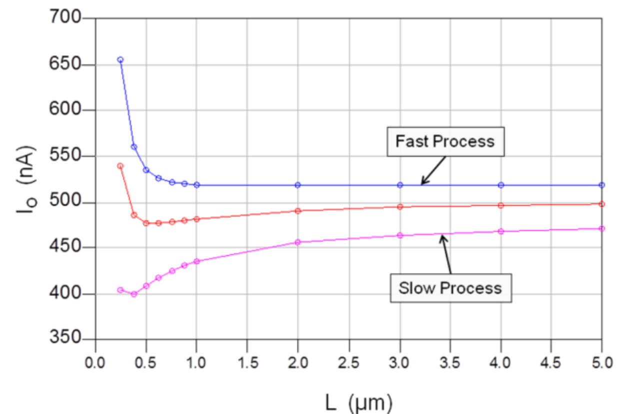

Fig. 6. I_0 vs L (channel length) and Process Corners (V_{DS}=1.8V).

Analog designers often refer to the "universality" of the transconductance efficiency versus inversion coefficient curve. To check how sensitive is such a curve to process corners, I_0 estimated results, that take into account adjustments of I_0 due to process corners, have been utilized to draw three such curves, nominal ,fast and slow, as shown in Fig. 7. The results presented in Fig. 7 substantiate the "universal" nature of the transconductance efficiency versus inversion coefficient curve as all three curves were shown to coincide.

The transconductance efficiency versus inversion coefficient curves shown in Fig. 8 are obtained from the identified I_0 values based only on the nominal MOS device. The results at the marker in Fig. 8 show that the g_m/I_D value has a 1.5% error for the slow device and 0.95% error for the fast device if one

uses the nominal I_0 value. In most design applications this is an acceptable error.

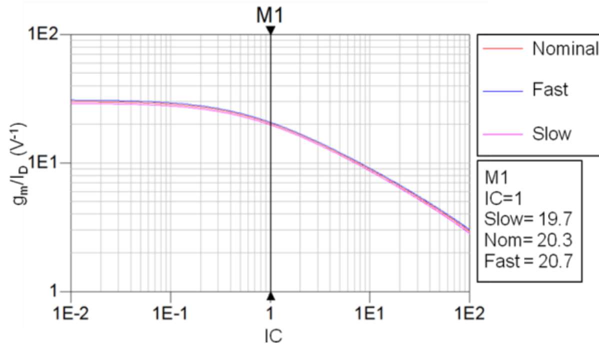

Fig. 7. g_m/I_D and Process Corners (L=4 μm and V_{DS}=1.8V) using correct I_0 for each process corner

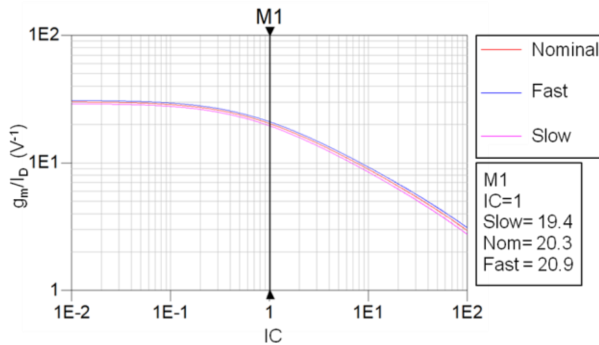

Fig. 8. g_m/I_D and Process Corners (L=4 μm and V_{DS}=1.8V) using I_0 from Nominal Process.

V. Example CS Amplifier using a Constant I_0 taken from a Long Channel MOSFET

In previous sections we explored the dependence of I_0 on V_{DS}, L and process corners. A simple example of a NMOS common source amplifier with a PMOS current source load is presented to further explore whether it is justified to assume a constant value of I_0 (based on experiments with a long channel MOSFET) in contrast to working with the I_0 vs. V_{DS} and L "look up" curves to adjust the I_0 values. For this example let us set L_{NMOS} = 0.25 μm, and L_{PMOS} = 0.5 μm. The intention is to show that the pre-design predicted gain matches the post design simulated measurement. The design of CMOS amplifiers often starts by partitioning the available DC supply voltage (V_{DD}) among all the transistors that share the same I_D. Let V_{DD} = 2.5V and assign V_{DSn} = 1.3V and V_{DSp} = 1.2V to assure that each of the transistors is in saturation.

The gain formula for the NMOS common source with PMOS current source load amplifier [7 chap. 3] is:

$$A_v = -g_{mn}\left(r_{dsn} \| r_{dsp}\right) \tag{5}$$

where g_{mn} is the NMOS transconductance, r_{dsn} is the NMOS drain to source resistance, and r_{dsp} is the PMOS drain to source resistance. This gain formula is a general networks theory theorem result [7] that is independent of MOSFET technology and model choice. An alternate way of representing the NMOS common source with PMOS current source load small signal voltage gain is:

$$A_v = -\frac{g_{mn}}{g_{dsn}+g_{dsp}} = -\frac{g_{mn}}{I_D}\cdot\frac{1}{\frac{g_{dsn}}{I_D}+\frac{g_{dsp}}{I_D}} \tag{6}$$

where I_D is the amplifier drain quiescent current. Equation (6) provides the gain of the amplifier in terms of the transconductance efficiency of the driving NMOS and the output conductance (g_{dsn}+g_{dsp}) normalized by the drain current. These entities graphs with respect to IC can be readily found from the design kit models via basic AC simulation or measurement in the laboratory once I_0 values for NMOS and PMOS transistors are determined. The measurement of g_{ds} involves placing a transistor on a schematic with a V_{GS} DC voltage source in series with an AC source. Both DC and AC analyses are needed. The AC analysis measures the AC drain voltage and is performed at a low enough frequency such that the internal transistor capacitors are essentially negligible whereas the DC analysis allows for the measurement of the quiescent drain current.

The output conductance of a MOS transistor depends on the drain to source DC voltage (V_{DS}), Inversion Coefficient (IC) and channel length (L) [6]. The simulation of the transistor has to therefore be performed for a specific set of V_{DS}, IC and L values.

In general NMOS common source with PMOS current source load amplifier design to meet multiple design specifications is accomplished by searching for values of IC, L, I_D and V_{DS} for each transistor . The unknown design parameters V_{GS} and W for each transistor are dependent on the design parameters used in the search. The search is not blind as it is guided by Binkley's operating plain.

In the example studied in this paper the only specification is the small signal voltage gain computed using (6) and design parameters selected as shown in Fig. 9. Selection of the aforementioned design parameters for each amplifier transistor has been set up in ADS such that by moving a series of sliders (see Fig. 9) the designer can immediately observe the voltage gain as determined by the four design unknowns and assess various design tradeoffs.

The NMOS Common Source amplifier with PMOS current source load amplifier requires that both transistors have the same I_D value therefore only one slider is needed for the current. The remaining parameters (i.e. L, V_{DS} and IC) do not have to be the same for both transistors hence a slider for each transistor.

The two gate to source voltages (V_{GSn} and V_{GSp}) values that were determined do not take into consideration such effects like the lateral side diffusion or any channel width dependency on the threshold voltage. In order to finalize the design a simulation of the final design is done in order to "fine tune" the values of V_{GSn} and V_{GSp} to make the design consistent with the design requirements for V_{DS} and I_D (the values for both V_{DS}

and I_D are from Fig. 10). The final values are V_{GSn}=0.464V and V_{GSp}=0.439V and the gain was 43.9 V/V, which are all in very good agreement with those shown in Fig. 10.

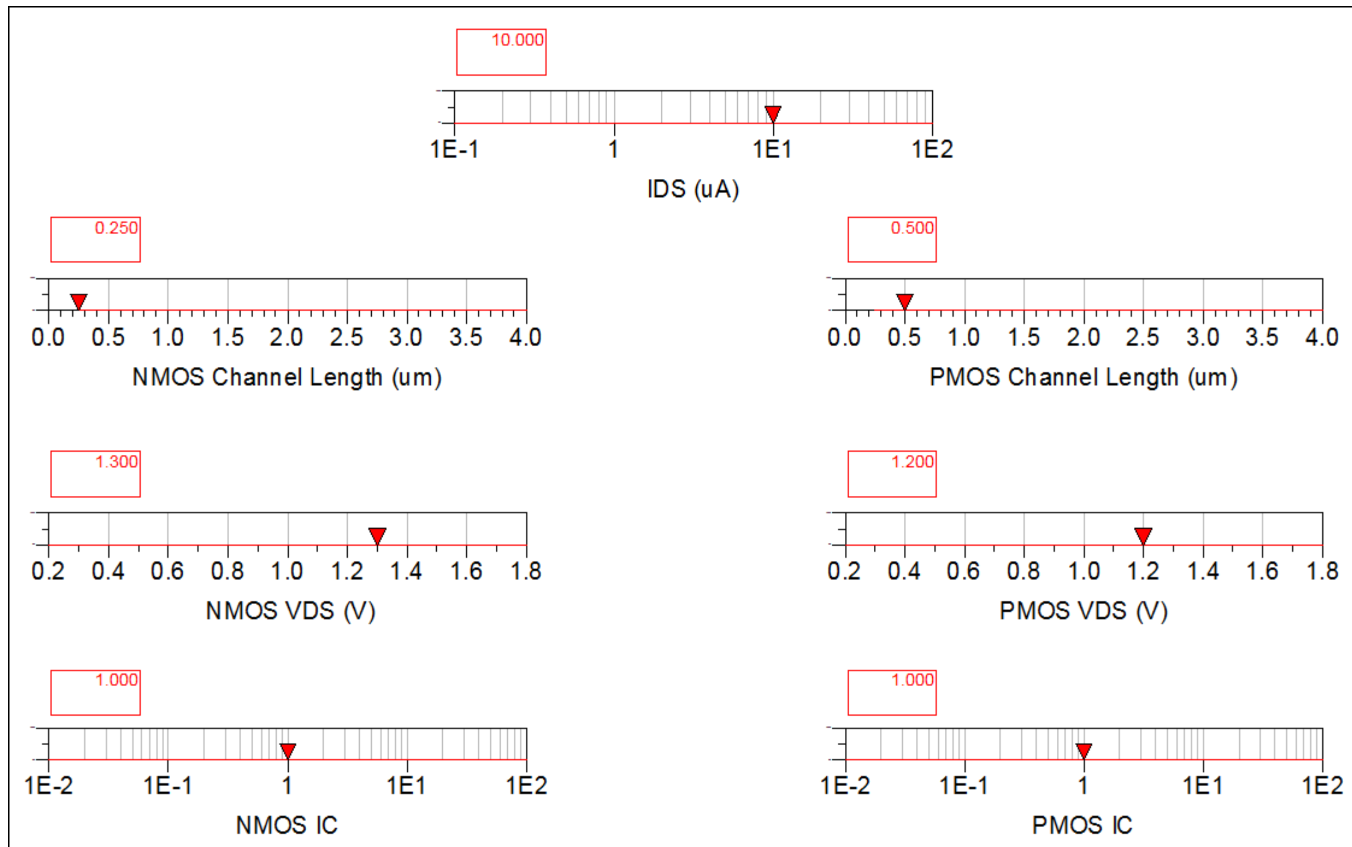

Fig. 9. User Interface Setup for NMOS Common Source with PMOS Current Source load Amplifier Design

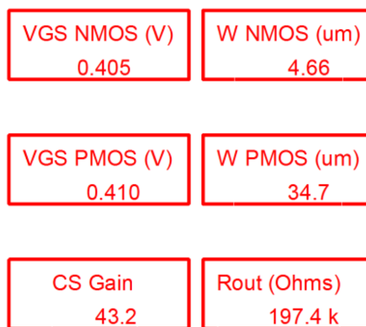

Fig. 10. NMOS Common Source with PMOS Current Source load Amplifier Design Parameters, Gain and Output Resistance (R_{OUT}).

VI. Example: Incorporating Process Tolerances into the Amplifier Design Process

One advantage of using a Design Kit from a semiconductor foundry (e.g. TowerJazz) is that process tolerances (represented by the fast/slow corners) may be taken into account during the design process as long as the foundry supports corner models. In the following experiment done on the circuit designed in the previous section both transistors are assumed to be having the same type of corners (either fast or slow), i.e. the fast-slow and slow-fast corner combinations are not considered practical. This approach is justified because in the actual process the NMOS and PMOS variations are not independent of each other [see 5 § 14.3]. Table 1 shows the estimated values for the amplifier's voltage gain, transconductance efficiency of each transistor and the current normalized drain to source conductances (g_{ds}/I_D) for the process corners. The estimated gain was obtained by direct application of equation (4).

For this experiment the amplifier was designed as per Fig. 10. The simulated measured gain matches the design value to within 2.1%. (due to such effects like the lateral side diffusion, channel width dependency on the threshold voltage, etc.). Note how the slow/fast simulated drain bias current drastically changes from that of the nominal process. The slow process has a lower current and therefore the Inversion Coefficient of both transistors is lower which explains why the gain went up (i.e. the lower IC the higher g_m/I_D). For the fast process the

current goes up which results in a high IC and hence a lower gain.

TABLE I
DESIGN SUMMARY BASED ON DESIGN SELECTION FROM FIG. 12. TAKING INTO ACCOUNT PROCESS CORNERS.

Process Corner	Slow	Nominal	Fast
I_D uA (simulated to test the design)	1.78	10	36
$(g_m/I_D)_N$ V^{-1}	26.60	21.89	14.52
$(g_{ds}/I_D)_N$ V^{-1}	0.427	0.396	0.338
$(g_{ds}/I_D)_P$ V^{-1}	0.055	0.111	0.132
IC (NMOS/PMOS)	0.10/0.14	1/1	3.87/4.19
Gain (estimated using sliders)	55.2	43.2	30.9
Gain (simulated to test the design)	50.3	43.9	32.5

As shown in section IV the value of I_0 varies with V_{DS} and L. The above amplifier design was performed allowing I_0 to adapt as we changed V_{DS} and L. However the impact of adapting I_0 is not as critical as observed all the way down to 0.25 µm in our studies so far. In another design experiment the value of I_0 was kept constant and the design proceeded in a very similar fashion. The values used for I_0 were based on those measured at V_{DS}=1.8V and L=4µm, that is I_0(nmos)=506.7 nA and I_0(pmos)=126.7 nA. The design setup shown in Fig. 10 was used and the results are shown in Fig. 11. After running ADS and fine tuning the values of V_{GS} for both transistors the final values obtained were V_{GSn}=0.461V and V_{GSp}=0.433V and the gain was 44.7V/V which are all in very good agreement with those shown in Fig. 11. The results of this experiment are shown in Table II and follow closely those of section V and show that using a unique long channel value for I_0 for NMOS and PMOS devices is a proper choice.

VGS NMOS (V) 0.415
W NMOS (um) 4.93
VGS PMOS (V) 0.416
W PMOS (um) 39.5
CS Gain 44.0
Rout (Ohms) 198.2 k

Fig. 11. NMOS Common Source with PMOS Current Source load Amplifier Design Parameters, Gain and Output Resistance (R_{OUT}) with Fixed I_0

TABLE II
DESIGN SUMMARY BASED ON DESIGN SELECTION FROM FIG. 11 WITH FIXED I_0 (I_0(NMOS)=506.7 nA AND I_0(PMOS)=126.7 nA).

	Slow	Nominal	Fast
I_D uA (simulated)	1.74	10	37.2
$(g_m/I_D)_N$ V^{-1}	26.57	22.18	15.35
$(g_{ds}/I_D)_N$ V^{-1}	0.427	0.397	0.347
$(g_{ds}/I_D)_P$ V^{-1}	0.064	0.107	0.132
IC (NMOS/PMOS)	0.09/0.13	1/1	4.35/4.35
Gain (estimated using sliders)	55.3	44.0	32.1
Gain (simulated to test the design)	50.2	44.7	32.8

VII. CONCLUSION

The value of the technology current I_0 is central to the methodology that uses transconductance efficiency g_m/I_D for the design of analog CMOS circuits. The paper presents a simple search technique to determine I_0 and it can be used with either measured data or simulation data using any MOSFET model. The sensitivity of I_0 to V_{DS} and channel length was also studied and selection of a proper I_0 value is important for a proper estimation of g_m/I_D vs. IC. An exact adjusted value of I_0 proved not to be essential to the design of a Common Source amplifier studied and a fixed I_0 value based on a long channel device can be used fairly effectively. Our simulation studies confirmed that MOS transistor transconductance efficiency vs. inversion coefficient curve shows little sensitivity to MOSFET process corners.

ACKNOWLEDGMENT

The authors wish to thank TowerJazz for providing the CA18HB process design kit (PDK) that was used in our research for all ADS analyses and simulations.

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BIOGRAPHIES

Wilfredo Rivas-Torres received his B.S.E.E. from Universidad Politecnica de Puerto Rico (UPPR), Hato Rey, Puerto Rico in 1988 and his M.S.E.E. from Florida Atlantic University, Boca Raton in 2004, where he is currently pursuing his Ph.D. degree in Electrical Engineering.

Zvi S. Roth received his B.Sc (1974) and M.Sc (1979) in Electrical Engineering from the Technion Israel Institute of Technology, and his Ph.D. in Systems Engineering (1983) from Case Western Reserve University. He joined Florida Atlantic University, Boca Raton, Florida in 1982, and is presently a Professor of Electrical Engineering and Associate Chair of the Computer and Electrical Engineering and Computer Science department. Dr. Roth's teaching and research interests include analog electronics design incorporating electronic simulation as an active design tool.