**Ravi Shankar**

**1. Contact Information**

Director, Center for Systems Integration (CSI)

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Web Links:

* Faculty Profile: <http://faculty.eng.fau.edu/shankar/>
* Google Scholar: <http://scholar.google.com/citations?user=4nMakAEAAAAJ&hl=en>
* Research site for the Center for Systems Integration: <http://csi.fau.edu/>
* Teaching: <http://android.fau.edu/> , <http://robotics.fau.edu/> , and <http://semanticweb.fau.edu/>
* eLearning Faculty Team Site: <http://eteams.pbworks.com/>
* Github Open Source App site (being developed): <https://github.com/RShankar?tab=repositories>
* Other: <https://www.linkedin.com/in/shankar2015> , & <http://www.researchgate.net/profile/Ravi_Shankar55>

My recent **research and teaching** focus: Semantic Web, STEM Education, Health Care, Mobile and Embedded Systems, Biomedical Engineering, and Systems and Software Engineering

**2. Professional Information**

**2.1. Educational Background**

* Data Science Certificate (non-credit), Johns Hopkins Univ., Baltimore, MD, Completion: Oct 2015 An online 10-course coursera sequence on data analytics; completed 7 courses (distinction), Signature Track; <https://www.coursera.org/specialization/jhudatascience/1?utm_source=catalog>
* Continuing Education Certificates in mobile learning and Web 2.0 tools from the Sloan Consortium (<http://onlinelearningconsortium.org/>) and in eLearning Facilitation from FAU (<http://www.fau.edu/cel/index.php>) , 2012-14.
* MBA College of Business, Florida Atlantic University, Boca Raton, FL, May 2000

Business Plan and New Product Development: PC-Based Hands-On Science Education for K-12 students.

* Ph.D. Electrical and Computer Engineering, University of Wisconsin, Madison, 1982.

Thesis topic: "The Origin of Impedance Pulse in the Limbs and Arterial Compliance Studies with Impedance Plethysmography." Specialization: Biomedical and Computer Engineering

* M.S. Electrical and Computer Engineering, University of Wisconsin, Madison, 1977.

Thesis topic on Cell Electrophoresis

* B.S. Telecommunication Engineering, Karnataka University, India, 1971.

**2.2 Employment History**

* **December 1993 – Present,** *Director, CSI,*

Center for Systems Integration (**CSI**)isa college-wide center for multi-disciplinary university-industry collaboration. Built a state-of-the-art facility with industry parallel tools and methodologies. Total funds obtained in the **Systems and VLSI** area: **$2.384 M** in federal and industrial cash grants (total inclusive of biomedical engineering and royalties: **$4.334 M**; and $57 M in industry in-kind contributions (from 1982 to 2008).

* **August 1991 – Present,** *Professor, CEECS* *(Computer and Electrical Engineering and Computer Science)*, Florida Atlantic University, Boca Raton, FL, Employer: Dr. Nurgun Erdol, Chair and Professor, Computer and Electrical Engineering and Computer Science Department, Ph: (561) 297-3486, Email: erdol@fau.edu
* **August 2012- May 2013,** *Sabbatical,*

Focus: Build multi-college collaborations in teaching and research and use my backgrounds in automation, productivity, entrepreneurship, medicine, eLearning and several application domains (smart phones, robotics and the semantic web) to develop open source tools to facilitate teaching, research and community needs, and to create opportunities for our graduates

* **August 2005- May 2006,** *Sabbatical*,

Focus: Motorola’s OPP (One Pass to Production) Project. Motorola Grant Through FAU. Sixth year of a eight year two million dollar project funded at about $1.06 M so far by Motorola (included above). I am the technical lead and the PI (Co-PI for the second year) for the project.

Motorola Sponsor: Mr. Jaime Borras, Corporate VP and CTO, iDEN, Motorola, Plantation, FL, Ph: (954) 723-3797, Email: Jaime.Borras@motorola.com

* **July 2002 – December 2002,** *Leave of Absence from Cadence at FAU*
* **January 2001- July 2002,** *Senior Consultant, Leave of Absence from FAU at Cadence,*

Cadence Design Systems. Addressed Long-range issues in design flow, tool integration, training, and learning, to enhance design and verification productivity. Collaboration with Motorola, S. Florida sites. Result: 8-year OPP Project (see above)

Employer: Lane Lewis, Motorola Enterprise Account Manager, Cadence Design Systems, Inc., Ph: (847) 284- 4729, llewis@cadence.com

* **May 1998 –August 1999,** *Sabbatical,*

Developed the infrastructure for rapid prototyping of biomedical, educational (K-12) and other systems. Two multi-year, multi-disciplinary, multi-institute proposals worth $16 M submitted in these areas. Result: Not funded. Started my Executive MBA.

* **May 1992 - May 1993,** *Sabbatical,*

Accelerated Product Development; Biomedical Imaging for Atherosclerosis

$750K + funding, sponsored by Vasocor Inc. Result: $1M in royalties to FAU from research commercialization. Total funds to FAU in the **biomedical** area: **$ 0.95 M** in cash grants and **$1M** in royalties (cash).

# August 1991 – 2002,  *Consultant*,

Vasocor. Topic: Biomedical Engineering, related to licensed atherosclerosis research.

* **August 1986 – 1991,** *Associate Professor*

Electrical and Computer Engineering, Florida Atlantic University, Boca Raton, Florida.

* **August 1986 – present,** *Consultant,*

IBM, APTEK, Harris, and Motorola. Topic: Engineering CAD tools and methodologies for digital and mixed mode design, simulation, synthesis, layout and test as applied to communication products.

* **August 1982 – 1986,** *Assistant Professor*

Electrical and Computer Engineering, Florida Atlantic University, Boca Raton, Florida.

* **May 1977 - May 1982,** *Teaching and Research Assistant*,

Electrical and Computer Engineering, University of Wisconsin, Madison, Wisconsin.

* **September 1971 - December 1973,** *Research and Development Engineer*,

Analog Design Group, Computer Division, E.C.I.L., Hyberabad, India.

**3. Instructional Experience**

**3.1 Courses Taught:**

* **Focus (2008-on) – Mobile Applications:** Software-Hardware CoDesign with Android, Android Components, Android Projects (on Robotics), Semantic and Intelligent Web Applications, all focused on various aspects (applications, frameworks, components, physical computing, graphics and animation, web services, and optimization) of the open source Android mobile platform of Google. Most courses are interdisciplinary with professors and students in other colleges.
* **Focus (2000- 2007) - System on a chip (SoC):** Network on Chip, Concurrency Modeling, Software-Hardware CoDesign, Computers as Components, CAD-Based Computer Design with SystemC, andSOC Design and Verification. Fall ’08: Biologically Inspired Architectures.
* **Focus (1999 – on) – Innovation:** New Product Development, College of Business, co-taught.
* **Focus (1986-1999) - VLSI:** Microelectromechanical Systems (with Dr. Masory); Analog and Neural VLSI; VLSI and Computer Architecture; Advanced Topics in VLSI Design (Low Power Design, SOI); Structured VLSI Design; Introduction to VLSI
* **Focus (1982-1992) – Architecture:** Embedded System Design I; Concurrent Processing (with Dr. Fernandez); Introduction to Neural Networks; Introduction to Microcomputers; Digital Computer Architecture I and III
* **Focus (1985- 2000) – Engineering Design Automation** - CAD-Based Computer Design (with Verilog and ARM); Structured Digital Design; Computer Hardware Design I and II; Semi-custom VLSI Design in DSP (with Dr. Sudhakar);
* **Focus (1982-1985): - Data Acquisition**: Data Acquisition and Measurement Systems; Biomedical Instrumentation Lab (U. of Wisconsin-Madison)
	1. **MS Theses Supervised**
* **Current:**

Aguerrevere, S., Optimization of QOS (Quality of Service) Metrics for a Low Cost Robot

Augustin, M., Math lessons with a Low Cost Robot

Serrano, M., Sentimental Analysis from Twitter Feeds

Terrell, D., Semantic Web for Interpretation of Crime Statistics

* **Languages:** Vo, T., Martial Arts as a Markup Language, August 2014
* **Systems:**

Islam, S., A Modeling Methodology for an RTOS, May 2007

Jain, A., Software Decomposition for Multicore Architectures, May 2006

Jillellamudi, H., “Modeling Multiple Abstraction Levels in SoC Using SystemC,” Dec 2003

Ajmera, A., “High Speed Scaleable Multiplier,” December 2003

Karnati, R., “Survey of Design Techniques for Signal Integrity,” December 2003

Reddy, J., “ Model to analyze interferences to a Bluetooth system,” May 2001.

Mandadi, S., “Operating System on a Chip: Implementation of Interprocess Comm.,” Aug 2000

* **VLSI and EDA:**

Riches, J., “Sigma -Delta Modulation, Low Power”, with Dr. Erdol (Co-Advisor), April 1999

Renavikar, A., "VLSI-Implementation of a Digit Classifier", July 1996

Madabushi, V., "A CCD-Array for Character Recognition", March 1995

Banuru, P., "FPGA (XILINX) Implementation of Feature Extraction Algorithm", Dec. 1994

Phadnis, M., "VHDL Modeling of a Character Recognition System", Dec. 1994

Du, J., "WSI for Alopex: Design and Test", April 1994

Xiao, Kang, "DCVS Logic Synthesis,” Co-Advisor, December 1992.

* **Architecture:**

Martin, G., "Character Recognition with Alopex", August 1992

Zhang, W., "VLSI-Implementation of a Parallel Thinning Algorithm", August 1992.

Bidari, R., "68000 Microprocessor-based System for Digit Recognition", August 1992

Freytag, L., "HDL Simulation and Digital Implementation of Alopex Neural Network," December 1990.

Pesulima, E.E., "Digital VLSI Implementation Issues of Artificial Neural Networks," August 1990.

* **Biomedical:**

Urso, A., "High S/N Ration Impedance Plethysmograph,” May 1990

Hernandez, L. "A Microprocessor Based Drug Infusion Control System,” Dec 1987.

Cikikci, I., "A Data Acquisition and Processing System for the Study of Peripheral Vascular System," December 1986.

* **Earlier:**

Chenthankij, A., "Digital PCM MF Receiver," May 1987.

Given, R.E., "A VLSI NMOS Implementation of a Building Block Processor using CORDIC Algorithms", August 1985.

Poenateetai, V., "Semi-Custom Design of Microprogrammed Testable Reduced Instruction Set Computer", April 1985.

**3.3 Ph.D. Dissertations:**

* Islam, S., An Adaptive Learning System to Increase STEM Interest, Expected to graduate in Dec 2015
* Wissinger, F., Infrastructure to model complex systems – hydrological modeling, Dec 2014
* Agarwal, A., QoS Driven Communication Backbone for NOC Based Embedded Systems, December 2006
* Suryaprasad, J., “SHINE: An Integrated Environment for Software Hardware,” December, 2003.
* Callaway, E., “A communication protocol for wireless sensor networks,” May 2002
* Horvath, E., "VLSI Placement," August 1992.
* Kolluri, S., "Early and Noninvasive Detection of Atherosclerosis," December 1991.
* Agba, L.C., "A VLSI-Implementation of Handwritten Digit Recognition Using Artificial Neural Networks," August 1990.
* Karralli, O., "A Very High Performance Neural Network System Architecture Using Grouped Weight Quantization," December 1989.

**4. Scholarly Achievements**

**4.1 Statement of Professional Interests:**

Semantic Web, STEM Education, Mobile Apps, Internet of Things, Biomedical Engineering, Software Engineering, Engineering Productivity, Concurrency, VLSI and EDA, and Computer Architecture

**4.2 Publications**

**4.2.1 Patents**

* Shankar, R., Pulsatile measurement of cardiac malfunction conditions, US Patent No. 8,197,416, Granted in June 2012
* Shankar, R., Noninvasive glucose measurement, US Patent No. 8,185,182, Granted in May 2012
* Shankar, R., [A Dynamically Reconfigurable Power-Aware, Highly Scalable Multiplier with Reusable and Logically Optimized Structures](http://www.csi.fau.edu/download/attachments/327/Dynamically%2Breconfigurable%2Bpower-aware.pdf?version=1), US Patent No. 7,873,823, Granted in January 2011
* Shankar, R., [High Speed Scalable Multiplier](http://www.csi.fau.edu/download/attachments/327/High%2Bspeed%2Bscaleable%2Bmultiplier.pdf?version=1), US Patent No 7080114, Granted in April 2006.
* Shankar, R., [Method of concurrent visualization of module outputs of a flow process](http://www.csi.fau.edu/download/attachments/327/Method%2Bof%2Bconcurrent%2Bvisualization.pdf?version=1), US Patent Application No. 20050010598. Published January 2005.
* Shankar, R., Method and Apparatus for Detecting the onset and relative degree of atherosclerosis in humans, International Patents, PCT claims (15), 1995. Expired due to non-payment of maintenance fees.
* Shankar, R., [Apparatus for Detecting the onset and relative degree of atherosclerosis in humans](http://www.csi.fau.edu/download/attachments/327/Method%2Band%2Bapparatus.pdf?version=1), 19 claims, USA Patent No. 5,343,867, Granted September 6, 1994.
* Shankar, R., [Method for Detecting Atherosclerosis while excluding motion artifacts](http://www.csi.fau.edu/download/attachments/327/Method%2Bof%2Bdetecting%2Batherosclerosis.pdf?version=1), 18 claims, USA Patent No. 5,297,556, Granted March 29, 1994.
* Shankar, R., [Early and Noninvasive Detection of Atherosclerosis](http://www.csi.fau.edu/download/attachments/327/Method%2Bfor%2Bdetecting%2Bthe%2Bonset.pdf?version=1), 25 claims, USA Patent No. 5,241,963, Granted Sept. 7, 1993.

**4.2.2. Journal Publications**

* Mitsova, D., Wissinger, F., Esnard, A-M, Shankar, R., and Giles, P., A Collaborative Geospatial Shoreline Inventory Tool to Guide Coastal Development and Habitat Conservation, ISPRS Int. J. Geo-Inf., **2013**, *2*(2), 385-404; doi:[10.3390/ijgi2020385](http://dx.doi.org/10.3390/ijgi2020385)
* Fonoage, M., Cardei, I., and Shankar, R., Mechanisms for Requirements Driven Component Selection and Design Automation, IEEE Systems J, Vol. 4, No. 3, Sept 2010, pp. 396-403
* Shankar, R., Gopinathan, M., and Webster, J.G., Digital Signal Processing in clinical validation studies with impedance plethysmography, Paper draft, CSI Technical Report, *csi.fau.edu*.
* Shankar, R., Shao, S.Y., and Webster, J.G., A Fully Automated Multi-Channel Digital Electrical Impedance Plethysmograph, Paper Draft, CSI Technical Report, *csi.fau.edu.*
* Shankar, R., Webster, J.G., Object-Process Modeling of Glucose Metabolism in Health and Disease, Paper Draft, CSI Technical Report, *csi.fau.edu.*
* Agarwal, A., Shankar, R., and Iskander, C.,Survey of NoC Architectures and Contributions, *Scientific International Journal of Engineering Computing and Architectures*, Vol. 3, Issue 1, 2009
* Agarwal, A., Shankar, R., A Concurrency Model for Network on Chip Design Methodology, *Journal of Modeling and Simulation*, Vol. 29, Issue 3, pp. 238-247, 2009
* Agarwal, A., Mustafa, M., Shankar, R., Pandya, A.S., and Lho, Y., A Deadlock Free Router Design for Network on Chip Architecture, *Journal of Korea Institute of Maritime Information and Communication Sciences*, Vol. 11, No. 4, pp. 696 - 706, April 2007
* Shankar, R., Freytag, L., and Alon, D., "A CAE-based Course for Design of Digital Systems: Details of a Tutorial Example," *Computers in Education* *Journal*, ASEE, Vol. 1, No. 3, pp. 76-85, July-September 1991.
* Zhongkai, Z., and Shankar, R, "A Tutorial on CMOS VLSI Design Useful for an Introductory Course," *Computers in Education Journal*, ASEE, Vol. 1, No. 3, pp. 22-30, July-September 1991.
* Shankar, R., and Webster, J.G., "Noninvasive Measurement of Compliance of Human Leg Arteries," *IEEE Trans. Biomed Eng.*, Vol. 38, No. 1, pp. 62-67, January 1991.
* Shankar, R., and Bond, M.G., "Correlation of Noninvasive Arterial Compliance with Anatomic Pathology of Atherosclerotic Nonhuman Primates, " *Atherosclerosis*, Vol. 85, pp. 37-46, December 1990
* Pajunen, G., Steinmetz, M., and Shankar, R., "Model Reference Adaptive Control with Constraints for Postoperative Blood Pressure Management," *IEEE Trans.* *Biomed. Eng.*, Vol. 37, No. 7, pp. 679-687, July 1990.
* Shankar, T.M.R., Webster, J.G. and Shao, S.Y., "The Contribution of Vessel Volume Change and Blood Resistivity Change to the Electrical Impedance Pulse," *IEEE Trans. Biomed. Eng*., Vol. BME-32, No. 3, pp. 192-198, March 1985.
* Shankar, T.M.R., and Webster, J.G., "Contribution of Different Sized Vessels in the Extremities to the Arterial Pulse Waveform as Recorded by Electrical Impedance and Volume Plethysmography," *Med. Biol. Eng. Comput.*, Vol. 23, pp. 155-164, March 1985.
* Shankar, T.M.R., and Webster, J.G., "Design of an Automatically Balancing Electrical Impedance Plethysmograph," *Journal of Clin. Eng*., Vol. 9, pp. 129-134, April-June 1984.
	+ 1. **Books**
* Agarwal, A., Shankar, R., and Pandya, A.S., Embedding Intelligence into EDA Tools to Meet the Future Technology Trends, Integrated Intelligent Systems for Engineering Design, Edited by Dr Xuan F Zha, National Institute of Standards and Technology, USA & Dr R. J. Howlett, University of Brighton, UK, UK, IOS Press, Amsterdam, Netherlands, 2006, pp. 389-408
* Shankar, R., and Fernandez, E., *VLSI and Computer Architecture*, 490 pages, Academic Press, Inc., August 1989.
	+ 1. **Refereed Conference Proceedings**
* Mitsova, D., Shankar, R., and McAfee, F., Mobile GIS Applications for Coastal Planning, accepted, *AESS 2015, (Assn for Environmental Studies and Sciences)*
* Islam, S., Shankar, R., Freytag, G., and Serrano, M., Empowerment with Informal Learning: Applicatrin of Mobile Technoloty to Teach Computer Science in K-12, *2nd International Conference on Microelectronics, Circuits and Systems, Micro2015*, August 2015, India.
* Shankar, R., Smart Phone Apps to Empower Middle School Students: Building a STEM Pipeline, *Twenty-Second International Conference on Learning*, The Learner Knowledge Community, Madrid, Spain, July 9, 2015
* Donate, K., Shankar, R., Mitsova-Boneva, D., McAfee, F., Searching the World Wide Web – Finding the Right Information the First Time, *122nd Annual ASEE Conference*, Seattle, WA, June 2015
* Shankar, R., Lapix, J., Ploger, D., Augustin, M., Weinthal, C., and Aguerrevere, S., Precision Low-Cost Robotics for Math Education Work In Progress, *122nd Annual ASEE Conference*, Seattle, WA, June 2015
* Shankar, R., Mentor and Mentee Pipeline in Smart Phone App Development, *2014 Annual Mentoring Conference*, at the Mentoring Institute, UNM, Albuquerque, NM, October 2014, presentation at: <https://prezi.com/usdx8fzhyq47/mentoring-pipeleine-smart-phone-apps/?utm_campaign=share&utm_medium=copy>
* Wissinger, F., Shankar, R., and Restrepo, J., Hydrologic Modeling Methodology, *IEEE SysCon*, Ottawa, CA, April 2014
* Carvalho, F., and Shankar, R., Biomedical Signal Processing: Designing an Engineering Laboratory Course Using Low-Cost Hardware and Software, *121st Annual ASEE Conference*, Indianapolis, IN, June 2014
* Shankar, R., McAfee, F., Harris, M., Behara, R., and Fowlkes, J., Android Exchange (AEx) - A Virtual Community for Students on eTeams, *EEE’13 -* Las Vegas, NV, July 2013.
* Shankar, R., McAfee, F., and Harris, M., Smart Phone App Development: A Multi-College Approach, *2013 Annual Conference, ASEE*, June 2013.
* Shankar, R., Dickson, J., and Mazoleny, C., A Tool for ABET Accreditation, *2013 Annual Conference, ASEE*, June 2013.
* Shankar, R., Ploger, D., Nemeth, A. and Hecht, S.A., , Robotics: Enhancing Pre-College Mathematics Learning with Real-world Examples, *2013 Annual Conf., ASEE*, June 2013.
* Islam, S., Shankar, R., and Freytag, G., Leveraging Semantic Web to Retrieve Customized Medical Information, *IEEE Syscon Conference*, April 2013.
* Ploger, D., Shankar, R., Nemeth, A., and Hecht, S.A., Exporting Engineering Technology Practice to Enhance Pre-College Mathematics Learning, Practice Brought Into the Engineering Technology Classroom, *2012 ASEE Gulf Southwest Annual Conf.*, April 2012 El Paso, Texas.
* Borras, J., Shankar, R., and Furht, B., Mobile Technology Consortium (MTC): An Industry-University Alliance, *Conf. on Industry and Education Collaboration*, Phoenix, AZ, Feb. 2013.
* Shankar, R., Borras, J., McAfee, F.X., Harris, M., Ploger, D., Masory, O., Behara, R., Impact of Motorola’s Vision on FAU’s Engineering Curriculum, *Conf. on Industry and Education Collaboration*, Phoenix, AZ, February 2013.
* Islam, S., Freytag, G., and Shankar, R., Intelligent Health Information System to Empower Patient with Chronic Diseases, *IEEE IRI Workshop on Health Informatics*, Las Vegas, August 2012.
* Mitsova, D., Esnard, A-M., Shankar, R., Wissinger, F. Viciedo, M., Holding Back the Sea: Approaches toward Shoreline Management and Planning to Reduce Erosion Hazards, Risk and Response: *Sea Level Rise Summit*, Ft. Lauderdale, FL, June 2012
* Shankar, R., Gundel, J., Nemeth, A., Ploger, D., and Hecht, S.A., Robotic Art for STEM, *FCRAR2012*, Boca Raton, FL, May 2012.
* Shankar, R., Ploger, D., Masory, O., and McAfee, F.X., Robotic Games for STEM Education, *ASEE Mid-Atlantic Regional conference*, Temple University, Philadelphia, PA, October 2011
* Shankar, R., McAfee, F., Carvalho, G., Silva, N., and Harris, M., STEM Education with Innovation and Entrepreneurship, *ASEE MidAtlantic Conference*, Temple University, Philadelphia, PA, October 2011
* Shankar, R., Preparing System Engineers of Tomorrow, *ASEE Southeastern Section Annual Conference*, Marietta, GA, April 5-7, 2009
* Shankar, R.,, and Agarwal, A., KISMET: An Open Source Process for Faculty Participation in ABET Accreditation, *ASEE Southeastern Section Annual Conference*, Marietta, GA, April 5-7, 2009
* Castellanos, R., Kalva, H., and Shankar, R., Low Power DCT using Highly Scalable Multipliers, *ICIP 2009*, Feb 2009.
* Fonoage, M., Cardei, I., and Shankar, R., , IEEE Systems Conference, 2009
* Jayadevappa, S., and Shankar, R., The Changing Ways of Computer Science & Engineering Education – A Suitable Pedagogy to Adapt Better, *2009 ASEE Annual Conference & Exposition*, Austin, TX, 6/15/09-6/17/09, Paper submitted: 2/6/09, 3/27/09
* Shankar, R., and Islam, S., A Reference Model Based Patient Management System: Opportunities and Challenges, *25th Southern Biomedical Engineering Conference* 2009, 5/15-17/2009,
* Mozelny, C., and Shankar, R., The Health Advisor: Application for Parkinson’s Disease, *25th Southern Biomedical Engineering Conference* 2009, 5/15-17/2009
* Agarwal, A., Iskander, C., Shankar, R., Hamza-Lup, G., System Level Modeling Environment: MLDesigner, *2nd Annual IEEE Systems Conference*, Montreal, Canada, April 2008
* Agarwal, A., Kalva, H., Iskander, C., Shankar, R., System Level Modeling in NOC Based H.264 decoder, *2nd Annual IEEE Systems Conference*, Montreal, Canada, April 2008
* Cardei, I., Fonoage, M., and Shankar, R., Model Based Requirements Specification and Validation for Component Architectures, *2nd Annual IEEE Systems Conference*, Canada, 2008
* Islam, S., Shankar, R., Agarwal, A., Katan, A., Iskander, C., Concurrency Compliant Embedded System Modeling Methodology, *2nd Annual IEEE Systems Conference*, Montreal, Canada, April 2008
* Hamza-Lup, G., Agarwal, A., Shankar, R., Iskander, C., Component Selection Strategies Based on System Requirements & Dependencies on Component Attributes, *2nd Annual IEEE Systems Conference*, Montreal, Canada, April 2008
* Shankar, R., Kalva, H., Agarwal, A., Jain, A., Annotation methods and Application Abstraction, *IEEE International Conference on Portable Information Device*, Orlando, FL, April 2007, pp. 1-5
* Mattu, B., and Shankar, R., Test Driven Design for Component Based Systems, *1st Annual IEEE Systems Conference*, Honolulu, Hawai, April 2007, pp. 25-31
* Choi, J., Islam, S., and Shankar, R., Unified Test Environment-Integrated Platform for Bridging the Modeling*, 1st Annual IEEE Systems Conference*, Honolulu, Hawai, April 2007, pp. 37-43
* Shankar, R., and Borras, J., Radical Productivity Improvement with One Pass to Production (OPP), *1st Annual IEEE Systems Conference*, Honolulu, Hawai, April 2007, pp. 85-92
* Cardei, I., Fonoage, M., and Shankar, R., M., Framework for Requirements-Driven System Design Automation, *1st Annual IEEE Systems Conference*, Honolulu, Hawai, April 2007, pp. 186-192
* Agarwal, A., Hamza-Lup, G., Shankar, R., and Ansley, J., An Integrated Methodology for QoS Driven Component Design and Component Selection, *1st Annual IEEE Systems Conference*, Hawaii April 2007, pp. 193-199
* Agarwal, A., Shankar, R., Kovalski, F., Modeling Concurrency on NOC Architecture with Symbolic language:FSP, *IEEE International Conference on Symbolic Methods and Applications to Circuit Design*, Firenze, Italy, Oct 2006
* Agarwal, A., Shankar, R., Modeling Concurrency in NOC for Embedded Systems, *IEEE Conference of High Performance Computing*, Massachusetts Institute of Technology, MIT Lincoln Labs, Boston, MA, September 2006
* Jain, A., and Shankar, R., Software Decomposition for Multicore Architectures, *High Performance Embedded Computing (HPEC) Workshop* at MIT Lincoln Laboratory, Boston, MA, 19 - 21 September 2006
* Selvan, V., and Shankar, R., “Comparison of Specification Languages and Tools,”, *UTC Telecom Conference*, Tampa, FL, May 2006.
* Freytag, G., and Shankar, R., “Assertion Based Verification,” *MEMOCODE* (Formal Methods and Models for Co-Design) Conference, Napa Valley, CA, July 2006.
* Shankar, R., and Barrett, R., Jr., “On Building a Long-Term University-Industry Collaboration,” *IEMC* (IEEE Engineering and Management Conference) 2005, Newfundland, Canada, September 2005
* Agarwal, A., Shankar, R., A Layered Architecture For NOC Design Methodology, *International Conference on Parallel and Distributed Computing and Systems,* November 2005 Phoenix, USA, pp.659-666
* Shurpali, P., and Shankar, R., “Concurrency Modeling,” *MSE* (Microelectronics Systems Education) Conference, San Jose, CA, June 2005.
* Asaduzzaman, A., Mahgoub, I., Kalva, H., Sanginepalli, Shankar, R., and Furht, B., “Cache Optimization for Mobile Devices Running Multimedia Applications,” *IEEE, 6th ISMSE*, Miami, FL December 2004, pp. 499-506.
* Jayadevappa, S., and Shankar, R., “CAD Based Design Course Using a State of the Art System Level Language,” American Society for Engineering Education (*ASEE*), Salt Lake City, Utah, June 2004
* Freytag, G., Shankar, R., “Digital Hardware Verification Methods, ” European Workshop on Microelectronics Education (*EWME*), poster paper, April 2004
* Shankar, R., and Jayadevappa, S., ““A New SystemC-based Foundation for the CE Curriculum,” European Workshop on Microelectronics Education (*EWME*), Oral Presentation, April 2004
* Jayadevappa, S., Mahgoub, I., and Shankar, R., Experiences of Modeling Soft IPs at High Level of Abstraction Using SystemC: A Case Study,” Design and Verification Conference (*DVCon*), San Jose, March 2004
* Jayadevappa, S., Shankar, R., and Mahgoub, I., “A Comparative Study of Modeling at Different Levels of Abstraction in System on Chip Designs: A Case Study,” IEEE Symposium on VLSI (*ISVLSI*), Lafayette, LA, February 2004
* Quraishi, G., and Shankar, R., “On simulating the IP Market Dynamics in an Academic Environment Using SystemC,” *MSE* (Microelectronics Systems Education) conference, San Jose, CA, June 2003
* Ajmera, A., Shankar, R., and Masory, O., “Behavioral Modeling with AMS Designer,” *BMAS* (Behavioral Modeling and Simulation) Conference, San Jose, CA, November 2002
* Ajmera, A., Masory, O., and Shankar, R., “AMS Designer for Mechatronics,” *International Cadence User Group Conference*, San Jose, September 2002.
* Rajeevalochanam, J., Suryaprasad, J., Shankar, R., et al., “High Performance modeling using VCC, ” *International Cadence User Group Conference*, San Jose, September 2002
* Shankar, R., “Concurrent Language for Capturing Chip Design Flow,” *International Cadence User Group Conference*, San Jose, CA, December 2001.
* Zhang, W., and Shankar, R., “A Parallel VLSI- Implementable Thinning Algorithm,” *Intl. Conf. on Parallel & Distributed Computing*, Orlando, FL, pp. 140-141, September 1995.
* Agba, L.C., and Shankar, R.," A Septon Feature Scheme in Handwritten Digit Recognition," *IJCNN*, 1992.
* Agba, L., Shankar, R., and Pandya, A., and Naylor, W.C., "A Handwritten Digit Recognition System," *Intl. Joint Conf. on Neural Networks*, January 1990.
* Pesulima, E., Pandya, A., and Shankar, R., "Digital Implementation of Issues of Stochastic Neural Networks," *Intl. Joint Conf. on Neural Networks*, January 1990.
* Shankar, R., and Bond, M.G., "Correlation of Noninvasive Arterial Compliance with Anatomic Pathology of Atherosclerotic Nonhuman Primates," poster paper 237, *8th Intl. Symp. on Atherosclerosis*, Rome, Italy, October 1988.
* Pajunen, G.A., Steinmetz, M., and Shankar, R., Model Reference Adaptive Control of Blood Pressure," *International Workshop on Adaptive Control Strategies for Industrial Use*, Lodge Kanaskis, Canada, June 1988.
* Shankar R., Cikikci, I.O., and Szabo, R., "A Biomedical Data Acquisition System," pp. 62, *22nd AAMI Annual meeting*, Los Angeles, CA, May 1987.
* Shankar, T.M.R., Bond, M.G., Gardin, J., and Wilmoth, S.," Noninvasive Compliance and Morphologic Data: An Animal Study," paper 46.3 39th *ACEMB*, Baltimore, MD, September 1986.
* Shankar, R., Ilyas, M. and Shamash, Y., "Evaluation and Implementation of CAD Work-stations in Electrical Engineering," pp. 714-717, 29th *Midwest Symposium On Circuits and Systems*, Lincoln, NE., August 1986.
* Shankar, T.M.R. "A Design Oriented Course on Computer Architecture," *Frontiers in Education Conference*, Philadelphia, PA, October 1984.
* Shankar, T.M.R., and Webster, J.G. "Noninvasive Determination of Arterial Volume-Pressure Curve," paper 41.5, *37th ACEMB*, Los Angeles, September 1984.
* Shankar, T.M.R., and Webster, J.G., "Measuring Arterial Volume-*Pressure* Characteristics using Impedance Plethysmography," *Vth Int. Cong. Elect. Bio-Imp*., pp. 307-310, Tokyo, August, 1981.
* Shankar, T.M.R., and Webster, J.G., "Design of an Automatically Resetting Electrical Impedance Plethysomograph," *IEEE Frontiers Eng. Health Care*, pp. 346-349, 1980.
* Shankar, T.M.R., and Webster, J.G., "Impedance Plethysmography for Early Detection of Atherosclerosis," paper 48.3., *Int. Conf. Med. Biol. Eng*. Jerusalem, 1979.
* Shankar, T.M.R., O'Neal, L.B., and Webster, J.G., "An Improved Cytopherometer," paper 48.6, *29th ACEMB*, Boston, 1976.

**4.2.5 Non-refereed Publications**

* Shankar, R., Suryaprasad, J., Mandadi, S., and Hsu, S., “Hardware Implementation of Rendezvous Inter-process communication with Round Robin Scheduling: Prototype of Two Processes,” KIE Conference, Japan, November 2001
* Shankar, R., and Masory, O., “A Cross-Disciplinary Course Sequence Useful for Microelectro-Mechanical Systems,” NSF Conference on ‘ Preparing the Leaders for Mechatronics Education’, San Francisco, CA, June 1996.
* Shankar, R., Korneluk, J., Patel, M., Martinez, M., and Masory, M., “Microcontroller-Based System Design: An Undergraduate Course for a Diverse Student Population,” NSF Conference on ‘ Preparing the Leaders for Mechatronics Education’, San Francisco, CA, June 1996.
* Gopinathan, M., Pulido, M., Szabo, B., Shankar, R., and Pajunen, G.A., "Computer Based Design of Stimulus Pattern Generator for Upper Arm Movement," *Robotic Conference*, FAU, Boca Raton, Fl, March 1992.
* Kolluri, S., and Shankar, R., "Noninvasive Determination of Atherosclerosis Using the Impedance Plethysmograph: A Longitudinal Study," *World Congress on Medical Physics and Biomedical Engineering*, Osaka, Japan, July 1991.
* Pajunen, G., Price, W., Shankar, R., and Smith, L., "On-Line Adjustment of Forearm Stimulus Pattern Based on Improved Nonlinear EMG Model," *Ninth Southern Biomedical Engineering Conference*, Miami, FL, November 1990.
* Kolluri, S., Shao, S.Y., and Shankar, R., "Data Acquisition and Control System for Monitoring Arterial Volume Change Signals Using a Multi-Channel Impedance Plethysmograph," *Ninth Southern Biomedical Engineering Conference*, Miami, FL, November 1990.
* Urso, A. Shankar, R., and Szabo, B., "An Electrical Impedance Plethysmograph for Recording from Small Arterial Beds," *Ninth Southern Biomedical Engineering Conference*, Miami, FL, November 1990.
* Landis, D., Athan, S., Brown, H., Sanders, T., Kozaitis, S., Shahsavari, M., and Shankar, R., "A Multi-function Wafer Scale System Architecture for Signal and Image Processing Applications," *Second Annual Florida Microelectronics Conference*, Melbourne, FL, pp. 21-24, May 1990.
* Pajunen, G.A., Price, W., Shankar, R., and Smith, L.E., "An Improved Nonlinear Model for On-line Application to Functional Electrical Stimulation," *American Control Conference*, May 1990, San Diego, CA.
* Pesulima, E.E., Shankar, R., and Pandya, A.S., "Digital Implementation of the Sigmoidal Transfer Function for Stochastic Neural Networks," *Second Annual Florida Microelectronics Conference,* Melbourne, FL, pp. 71-74, May 1990.
* Zhong, Z. and Shankar, R., "Design and Testing of an Analog Cell Library Useful for Artificial Neural Networks," *Second Annual Florida Microelectronics Conference*, Melbourne, FL, pp. 67-70, May 1990.
* Agba, L.C., Berthin, M. Miro, F., and Shankar, R., "A General Purpose Analog Neural Network Implementation", *Second Annual Florida Microelectronics Conference*, Melbourne, FL, pp. 63-66, May 1990.
* Shankar, R., Agba, C., Naylor, W.C., and Pandya, A., "Handwritten Character Recognition," *Southcon,* Orlando, FL, pp. 390-455, March 1990, Invited paper.
* Urso, A., Shankar, R., and Wagner, W.D., "Design of a High Signal to Noise Ratio Electrical Impedance Plethysmograph," *IEEE Southeastcon*, New Orleans, April 1990.
* Szabo, B., Szabo, R., Shankar, R., Urso, A, and Kolluri, S., "A Data Acquisition and Signal Processing System for EMG and Acceleration Signals," *IEEE Southeastcon*, New Orleans, April 1990.
* Zhongkai, A., Barrett Jr., R., Shankar, R., "An Analog Cell Library Useful for Artificial Neural Networks," *IEEE* *Southeastcon*, New Orleans, April 1990.
* Pandya, A., Shankar, R., Freytag, L., "An SIMD Architecture for Alopex Neural Network," *SPIE/SPSE Symposium on Electronic Imaging*, February 1990.
* Shankar, R., Agba, L.C., and Pandya, A., "Automated Handwritten Character Recognition with Artificial Neural Networks," *First Annual Florida Microelectronics Conference*, May l989.
* Shankar, R., Chentanakij, A., Muter, G., and Blashfield, W., "An Innovative Digital MF Receiver for PCM systems", *EE International Conference on Circuits and Systems*, Nanjing, China, July, 1989. Conference cancelled.
* Shankar, R., Freytag, L., and Alon, D.A., "A CAD-Based Course for Design of Digital Systems: Details of a Tutorial Example," *1989 IEEE Southeastcon Conference*, Columbia, SC, pp. 1404-1411, April 1989
* Hernandez, L. Shankar, R., and Pajunen, G.A., "A Microprocessor Based Drug Infusion Control System Employing a Model Reference Adaptive Control Algorithm to Regulate Blood Pressure in I.C.U. Patients," 1989 *IEEE Southeastern Conference*, Columbia, S.C., April 1989.
* Moller, H.C., Shankar, R., and Szabo, B., "Cross Correlation of Electromyographic (EMG) Signals from Consecutive Arm Movements," *1989 IEEE Southeastern Conf*., Columbia, S.C., pp. 1261-1263, April 1989.
* Agba, L.C., and Shankar, R., "A Novel Method for Pattern Recognition with Special Application to Alphanumeric Characters," *First Conference on Recent Advances in Robotics*, FAU, Boca Raton, FL, pp. 50-54, May 1988.

**4.3 Industry Final Reports And University Technical Reports**

* Shankar, R., Agarwal, A., Hamza-Lup, McAfee, F., and Silva, N., Accelerated Mobile Product Development – An Economic Engine for Science and Technology Superiority, SBA, Quarterly Reports, 9/09, 12/09, 3/10 and 6/10
* Shankar, R., Kalva, H., Iskander, C., Huang, S.,. and Mahgoub, I., One Pass toProduction, a collection of white papers and progress reports submitted to Motorola, February 2006 and earlier, 250+ pages. (all these will be published soon at ourwebsite: www.csi.fau.edu)
* Shankar, R., Mahgoub, I., VanHilst, M., and Furht, B., One Pass to Production, collection of white papers & progress reports submitted to Motorola, December 2004, 500 pages.
* Furht, B., and Shankar, R., White Papers: One Pass to Production, a collection of white papers & progress reports submitted to Motorola, June 2004, 250 pages.
* Shankar, R., and the OPP group, A Motorola Internal Website with details of our project presentations, paper summaries, demos, codes, etc., 2003.
* Callaway, E., Hsu, S., and Shankar, R., “JAN: A Communication Model for Wireless Sensor Networks,” Technical Report, TR-CSE-02-12, Dept. of Comp. Sci & Eng., Fla Atlantic University, February 2002.
* Callaway, E., Hsu, S., and Shankar, R.., “On the Design of Early Radiotelegraphic Wireless Networks,” Technical Report, TR-CSE-02-02, Dept. of Comp. Sci & Eng., Fla Atlantic University, February 2002.
* Freytag, L., and Shankar, R., “Structural Design of a Digital System,” A set of training videotutorials, Motorola, July 1996.
* Shankar, R., "End Points: Clinical Validation Studies with the Impedance Plethysmograph on Early and Noninvasive Detection of Atherosclerosis," Vasocor Internal Report, 20 pages, May 1994
* Shankar, R., Huang, Z., Parigie, E., and Madabushi, V., " A Noninvasive method for Objective and Repeatable Blood Pressure Measurement based on Impedance Plethysmography," Vasocor Internal Report, 70 pages, May 1994
* Shankar, R., Martinez, M., Prasanth, B., Nagaraja, P., Phadnis, M., and Barrett, R.., "Pattern Recognition: Automated Analysis of Arterial Volume Change with Cuff Pressure to Qualify the Extent of Atherosclerotic Disease," Vasocor Internal Report, 137 pages, May 1994.
* Gopinathan, M., Shankar, R., Kolluri, S., Nagaraja, P., Parigi, E., Desai, P., Martinez, M., and Huang, Z., "Digital Signal Processing in Clinical Validation Studies with Impedance Plethysmography," Vasocor Internal Report, 299 pages, March 1994
* Shao, S.Y., Shankar, R., Wu, M., Freytag, G., Wei, D., Liao, Y., Iyer, V., Kumar, D., Maharajh, N., and Ming, D., "Three Channel Impedance Plethysmography", Vasocor Internal Report, 109 pages, March 1994.
* Zhang, W., Shankar, R., and Barrett, R., "DCVS Testability Issues," Final report, IBM project, May 1991.
* Kang, X., Barrett, R., and Shankar, R., "DCVS Logic Synthesis,", Final report, IBM project, May 1991.
* Chentanakij, A., and Shankar, R., "Simulation Studies: A Digital MF PCM Receiver," Final report, APTEK project, May 1987.
* Shankar, R., Agba, L., Chentanakij, A., Hernandez, L., Sanville, P., "Base 2 and Base 3 Simulations," Final report, IBM project, September 1986.
* Shankar, R., Benayoun, R., Chentanakij, A., Sanville, P. "Design of a Bridge Adapter," Final report, IBM project, September 1986.

**4.4 Demonstrations/ Presentations / Posters**

* Shankar, R., Norona, C., and Gallego, V., Android at FAU, Presentation to MTC (MobileTechnology Consortium), February 2010, February 2011
* Shankar, R., Kalva, H., Huang, S., Iskander, C., Jain, A., Agarwal, A., Kovalski, F., Cruz, C., Patel, T., and Freytag, G., PI; Shankar, R., QTIP (Quarterly Technology Innovation Project) Demos (5) and Presentation (1), Motorola, November 2005
* Kreighoff, C., Tezak, T., and Freytag, G., PI: Shankar, R., QTIP (Quarterly Technology Innovation Project) Demos (2) and presentation (1) , Motorola, November 2004.
* Krieghoff, K., and Shankar, R., UML to SystemC, QTIP (Quarterly Technology Innovation Project) demo, Motorola, May 2004.
* Demos (5) and presentation (1) , PI: Shankar, R., SystemC, UML, and OPPflow, Quarterly Technology Innovation Project) presentations, Motorola,November 2003.
* Shankar, R., Barrett, R., La Vell, J., Freytag, L.,, and Durr, R., “A Framework for Multidisciplinary Collaboration,” Poster Paper, NSF Conference on ‘ Preparing the Leaders for Mechatronics Education’, San Francisco, CA, June 1996.
* Shankar, R., Freytag, L., La Vell, J., and Mazuera, O., “A Seamless Environment for Productivity Enhancement: HDL for Structured Design and Synthesis,” Poster Paper, 1996 NSF Design and Manufacturing Grantees Conference, Alburquerque, NM, January 1996. In the Proceedings: pp. 165-166.
* Horvath, E.I., Shankar, R., and Pandya, A.S., "A Parallel Algorithm for Standard Cell Placement," Poster paper, *intl. Joint Conf. on Neural Network*, June 1991.

**4.5 Reviews**

* Reviewer for the Annual ASEE Conference, 2013-2015
* Reviewer for the Annual IEEE Syscon Conference, 2013, 2015
* Reviewer for the Annual Mentoring Conference, 2014
* Reviewer for the IEEE Systems Journal and The Journal for Production Planning and Control, 2010
* Reviewer for two regional ASEE conferences in Austin, TX, and Marietta, GA; Also for journal papers on Supply Chain Management and Biomechanics - 2009
* Reviewer and Session Chair, 1st IEEE Systems Conference, Honolulu, Hawai, 2007
* Reviewer for JERIC, ACM, 2005
* Reviewer for the IEEE Transactions on Biomedical Engineering, 1992 – 1998
* Reviewer for Neural Networks, 1991
* Reviewer for the Test and Technology Committee, IEEE Computer Society., 1990
* Reviewer for IEEE Symposium on Parallel and Distributed Processing, July 1990.
* Reviewer for the ACM/IEEE Design Automation Conference, June 1988 - 94 (except 1990).
* Reviewer for the Proposals and Abstracts, Florida High Technology and Industry Council, 1988 – 1992
* Member, Balloting Committee, Design Automation Technical Committee, VHDL Analysis and Standardization Group, IEEE Computer Society, IEEE 32-bit microprocessor Sparc-based standard, 1993; Many Verilog HDL and VHDL standardization efforts, 1987 – 1997
* Reviewer for the *Eleventh and Thirteenth Annual Symposium on Computer Applications in Medical Care*, Washington, DC, November 1987, and November 1989.
* Reviewer for two articles in *Encyclopedia of Medical Devices and Instrumentation*, ed. J.G. Webster, Wiley International, 1987.

**5. Research**

**5.1 Sponsored Research (Cash Grants as PI - Total: $ 4.352 M**

 (Systems & VLSI: $ 2.402 M, Biomedical: $ 0.95 M, and Royalties of $1.0 M)

* Shankar, R., and McAfee, F. Citizen Science Apps, Grant from the Museum of Science $18,000

and Discovery, Ft. Lauderdale, FL, June 2015- August 2015

* Shankar, R., (PI), Voss, R., Ploger, D., Nemeth, A., McAfee, F. $20, 861

Integrating Mobile Apps and Robotics into STEM Education,

FAU Tech Fee Grant, October 2013

* Mitsova, D., (PI) and Shankar, R. (Co-PI), A Shore Zone Inventory/ $10,000

Characterization Tool as an extension to ARCGIS, funded by FAU’s

Sponsored Research, Start date: July 2012.

* Shankar, R., Lab Tech Fee Grant, to build Robots for a course, 3/11 $2,796
* Miranda, M., Undergraduate Research Grant from FAU, Mentor: Shankar, 2/11 $600
* Ploger, D., (PI), Shankar, R., McAfee, F., and Watson, T., (Co-PIs), Equipment

Grant, 4-G modems from Clearwire, to enhance multi-campus research, 12/10 $10,000

* Berry, L., (PI), Shankar,and others (Co-PIs), Rationale for Establishinga CCEP

Parternship, FAU, 5/10, on. No Specific funding allocation for Shankar

* Shankar, R., PI, Android App Development, 9/10-12/10, FAU $7,700
* Shankar, R (PI), Agarwal (Co-PI), Accelerated Mobile Product Develop-

Ment – An Economic Engine for Science and Technology Superiority, SBA

Grant, 9/09-8/10 $122,821

* GAP Funding from DSR/ OTT: Highly Scaleable Multiplier, 1/07-12/08 $15,000
* One Pass to Production, Motorola/iDEN 1/07 – 12/07 (PI, Co-PI: Furht $ 68,000

and Agarwal)

* One Pass to Production, Motorola/iDEN 1/06 – 12/06 (PI, Co-PI: Furht) $251,000

(Funding committed by Motorola at $250 K / year, through 2010. Long-term

commitment leveraged in many ways to be more productive. See cover letter)

* One Pass to Production, Motorola/iDEN 1/05 – 12/05 (PI, Co-PI: Furht) $185,000

(after subtraction of $25 K – For Six Sigma – Dr. Michael VanHilst is PI for that)

* Microprocessor Lab Upgrade, College of Engineering, April 2004 $10,543
* One Pass to Production, Motorola/iDEN, 1/04 – 1/05 (Co-PI, and Technical and Management Lead, PI: Furht) $250,170
* Exeuctable Process Flow, Motorola/iDEN, 2/03 - 12/03 (PI, Co-PI: VanHilst) $256,000

(same as: One Pass to Production)

* Cadence EDA Tool Acquisition Grant (two years, 2001-2003) $11,000
* Highly Scaleable Multiplier, Student Support, DSR, FAU (2002-2003) $3,000
* EDA Undergrad Curriculum –Cadence Design Systems, Inc (2001-2002) $20,000
* Low Power Optimization, SABA Grant, Motorola, PI, August 2000 – July 2001 $21,744
* Advanced Control Concepts in System Design, Motorola, PI, Co-PI: Pajunen

Motorola, January - April 1999 $72,000

* Integration of RF System Modeling with Digital Design Flow, Harris Semi $25,000

Conductors, PI, March 1997 - December 1997

* Acquisition of a Modularly Expandable Mixed Signal IC Tester, NSF, FAU, and

Motorola Funds, PI, June 1994 - July 1997 $259,047

* A Seamless Environment for Productivity Enhancement: NSF and Motorola

Funds, PI for one, Co-PI for another, June 1994 - April 1995 $84,632

* Early and Noninvasive Detection of Atherosclerosis: $750,000+

Clinical Validation, P.I., Product Center Corporation,

Vasocor, Miami, Florida, 1991-1993 (through 10/93)

* Character Recognition with Neural Networks, IBM, $85,700

Co-P.I. (P.I.: Dr. A.S. Pandya), 1990-1992

* Layout Topology Optimization for Enhanced Yield $77,000

Performance and Testability of DCVS Logic, IBM, P.I.,

(with Dr. R. Barrett, Jr.), 1990-1991

* Honorable Mention IEEE/ACM SIGDA DATC Grant $1,000

to Support DA Activities, P.I., 1990-1991.

* Wafer Scale Integration for Image Perception, P.I., $77,964

DARPA/SUS, 1989-1990

* VLSI Implementation issues relevant to hand-printed $109,323

character recognition with neural networks, P.I., (with 7

Dr. A.S. Pandya), Florida High Technology

and Industry Council, 1989-92

* Early Detection of Atherosclerosis, Dept. of Sponsored $27,000

Research, FAU, P.I., 1989-1990

* Patterned Functional Electrical Stimulation for $35,000

Restoration of Volitional Limb Movement in Hemiplegics,

P.I., (with Drs. G. Pajunen, B. Szabo and L. Smith)

Florida High Technology and Industry Council, 1989-90

* Design of Analog VLSI Cell Library, USF, $39,500

Tampa, P.I., 1986-1988

* VLSI Design of Communication Systems, APTEK, P.I. $75,000

(with Dr. R. Szabo), 1986-1987

* Early Noninvasive Detection of Atherosclerosis, Florida $133,000

Hi-Tech Council, P.I.: 1985-1987

* Purchase of a Daisy VLSI Design Station $10,000

FAU Equipment Grant

* Distributed Computing and VLSI Design, IBM P.I. $124,667

initially with Dr. Y. Shamash and Dr. L. Raskin, 1984-1986

* Early Detection of Atherosclerosis, Seed Grant $3,500

Florida Atlantic University, 1983-1984

**5.2 In-Kind Donations:**

 **To the Center for VLSI and Systems Integration, now known as**

 **The Center for Systems Integration:**

* CoWare Design Tool for software-hardware codesign, 2003 (expected)
* PC Donations, iDEN, Motorola, 2003 $ 5,000
* LDV – Cadence for mixed language simulation
* NT Server – Donation by Ligi Tool Inc., May 1997 $ 21,000
* Mentor Graphics - WorkFlow Expert and CVE for Emb.Dsgn, May ’97 $ 3.0 M (Est.)
* ARM Verilog Emulator and ARM development system, Jan ’98 $ 1.0 M (Est.)
* Silvaco for Process, Device and Circuit level simulations, May ’97 $ 3.5 M (Est.)
* Motorola, Infrastructural grants, May 1994 - present $285,000
* PowerMill from EPIC Design Automation Inc., March 1996 $ 1.5 M (Est.)
* Synopsys for High Level Synthesis, April 1996 $ 3 M
* Logical Devices, CUPL for PLD and FPGA design, January 1995 $7,990
* QuickTurn, Rapid prototyping systems, from IBM, January 1995 $307 K
* Cadence, Design, simulation and synthesis tools, August 1994 $36.8 M +
* Analogy, Mixed mode design and simulation tools, October 1994 $1 M
* Sun Harddisk (8.4 GB), from Motorola, March 1994 $9,500
* Cascade, Layout and synthesis tools, December 1993 $4.7 M

**Prior to December 1993 (Center Formation):**

* Xilinx Annual Maintenance (1993 - 94) $15,000
* Xilinx Training center, 1992 $34,600
* DSP56OOO Development System, Motorola, 1991 $4,600
* Artificial Neural Net Lab for Research and Teaching, Intel, 1991 $41,300
* IBM, Daisy Meglogician, May 1990 $150,000
* Sun, SparcStation 4/110, July 1990 $28,850
* IBM, PS/2 System, January 1990, Co-P.I. (P.I.: Dr. Pandya) $20,700
* IC Fabrication, NSF and MOSIS, 1987 – 1996 $50,000+

**6. Professional Service**

**6.1 Membership in Professional Societies**

* IEEE (Senior Member), and AHA (Fellow): 1982-2012,
* AMIA (2012-2014) and ASEE (2012-2014)

**6.2 Professional Registration**

* P.E. (Professional Engineer), State of Florida (1984-present).
* CITI (Collaborative Institutional Training Initiative) Certification for both Biomedical Research Investigators and Social & Behavioral Research investigators (September 2011-2017)

**6.3 University Service**

* ABET Coordinator for Computer Engineering – A softcopy document developed for the first time, based on the Motorola/OPP methodology, June 2008. Full ABET Accreditation received promptly.
* Academic Coordinator, MSTC (Master of Science in Technology Commercialization), a joint program developed by the colleges of science, engineering & computer science, and management, to help intrapreneurs and entrepreneurs with taking a concept to commercialization, Program Coordinator: Dr. Darab Unwalla, Professor Emeritus, College of Business, 2005-2006. Program withdrawn
* Mentor (unofficial) for 6 faculty members and 3 PhD Students to evolve a long-term FAU-Motorola relationship, 2003. Now, part of the Motorola OPP project team.
* Member, Executive Committee, Computer Science and Eingineering Department, 2003 – 2006, 2007- present.
* Director, Computer Engineering Undergraduate Committee, CSE, 2003-2005. and 2007-present. Results: updated the curriculum, Defined the CE discipline, Streamlined and added courses on systems engineering & made ABET On-Line feasible.
* Developed the proposal for a BS in Bioengineering, in collaboration with the EE, CSE, and ME faculty in the college of engineering, and the Biology department
* and CMBB (Center for Molecular Biology and Biotechnology) in the college of Science, July 1999.
* Organized several industrial presentations at FAU in 1993 from Cascade, Motorola, Logic Devices Inc., and Synopsys.
* Co-Chair, IC-Working Group, FAU-Motorola Collaboration, 1993- 1998. Not active at present.
* Member, Department Chair Search Committee, 1993, Committee Disbanded after the

department chose an internal candidate.

* Member, Maspar Acquisition Group (1992)
* Member, College Planning and Development Committee (1992-1993, 1994-1996)
* Member, Dean's Ad-Hoc Committee on Long Range Plan (1992)
* **Director, Center for** (VLSI and) **Systems Integration**, for multi-disciplinary research and teaching, involving CSE, EE and ME faculty members, Approved by the College of Engineering, April 1994. Facilitated strong support by Motorola and IBM ($57 Million in In-kind donations and grants); 3 NSF grants. Several of our students have joined Cadence, Motorola, Synopsys, Xilinx, IBM, Intel, & other high tech companies.
* Coordinated Engineering equipment needs for the new Engineering and Science Building, 1989
* Member, Organizing committee, Second Florida Microelectronics Conference, Melbourne, May 1990
* Coordinated the evolution of teaching lab and research facilities, and research projects in ECE, CE and CSE departments (1982-present) in the areas of VLSI, Neural Networks, System Integration, Testing, and Biomedical Engineering. These are multidisciplinary projects and have involved the following FAU faculty members: R. Barrett, G. Pajunen, A.S. Pandya, B. Szabo, and O. Masory.
* Organized the First Florida Microelectronics Conference, Boca Raton, May 1989 (with K. Lioy and R. Messenger)
* Department Representative, Library Committee (1982-1986)
* Member, Engineering College Minority Activities (1984-1985)
* Senator, University Senate, 1987-1989
* Chairman and Member, Department Lab and Equipment Committee (1985-1987, 1988-92)

**7. Professional Recognition**

* Shankar, R., MDA to Eclipse Modeling Framework, a workshop presented at IEEE Syscon Conference, Ottawa, CA, April 2014
* Shankar, R., and Islam, S., Semantic Web Technologies, a workshop presented at IEEE Syscon, Orlando, FL, April 2013.
* Member, Panel Discussion on Education Alternatives for Combining Engineering and Management, IEMC, Newfundland, September 2005
* Dean’s Faculty Award, Annual Award for Outstanding Faculty, College of Engineering, December 2003.
* Plaque of appreciation, Presented by Mr. Jaime Borras, Corporate VP and CTO, iDEN, Motorola, for leadership in implementing ‘One Pass to Production’ and ‘Digital Six Sigma’ program, September 2003.
* Leadership award, by Dr. Borko Furht, CSE Dept., FAU, for leading the department in establishing collaborative relationship with Motorola that has led to 3 grants and 3 potential grants to various faculty members, March 2003.
* Member, Panel Discussion on Education Alternatives in Biomedical Engineering, Biocomplexity Conference, Dartmouth, July 2002
* Team of the Year award to our Motorola Enterprise Team at Cadence Design Systems, Inc, January 2002. I was a senior member of the team.
* Session Chair, Grand Unification, First SMT Conference, Polytechnic University of Puerto Rico, Puerto Rico, November 1996
* Industry - University Collaboration, Round Table Discussion, Invited Participant, SouthCon, Ft. Lauderdale, FL, Spring 1995
* NSF and FAU/Manufacturing Engr. program - NSF workshop on Mechatronics, CalPoly, Summer 1995
* Motorola and Cascade sponsorship- Cell Generation for automatic retargeting to different technologies, Phoenix, AZ, Spring 1995
* Motorola sponsorship - University - Industry collaboration in mixed mode design, Analogy Conference, Livonia, MI, Fall 1994
* Invited to be editor of Intel's ETANN user group newsletter. Declined.
* Invited to be a member of Biomedical Engineering Subcommittee, Florida High Technology and Industry Council, 1990. Declined.
* Plaque presented by Drs. Barrett, Pandya, B. Szabo and R. Szabo in appreciation of hard work, guidance and leadership (September 1990).
* Member, Microelectronics and Materials Subcommittee, Florida High Technology and Industry Council, (1988-1992).

**8.**  **Other Information**

**8.1. Research Commercialization**

* FAU's first licensing contract based upon Dr. Shankar's research on Early and Non-invasive Detection of Atherosclerosis, signed March 1991. Royalty payments worth a total of $1 Million have been received by FAU Research Corporation through 2004 (same as the item mentioned under employment history).

**8.2. Continuing Education**

* Computational Investing, Part 1, Georgia Tech, Coursera course, Big data analytics with focus on investing using Python, November 2014
* Mobile Learning Mastery Series, February 21- April 25, 2014, from the Sloan Consortium
* Certificate of Achievement, Web 2.0 Tools You can Use to Improve Learning, Dec 2012, from The Sloan Consortium.
* eLearning Designer/Facilitator Certification at FAU, passed with honors, May 2012
* NIH, UMLS (Unified Medical Language System) 1-day training, Fall ‘07
* Rhapsody, UML Tool for Real-Time, Motorola Funding, FAU, April 2004
* NSF Sponsored Workshop on Biocomplexity, at Dartmouth College, Hanover, NH, July 2002.
* Leadership Training, 3 day certification course during my stay with Cadence, The Client Partner, Aspen Consulting Inc., April 2002.
* Position as Senior Consultant at Cadence, with focus in the area of SFV (Systems and Functional Verification), during January 2001 to July 2002. SFV is the major area of challenges for system design and integration in this SoC (System-on-a-Chip) era. Several papers and internal documents were prepared.
* Active support of Cadence tools and design flow, during January 2001 – present at Motorola. Significant experience.
* Design experience with UML, MLD, SystemC, Verilog, SPW, Cascade, Analogy, PSPICE, HSPICE, Matlab, HP Tester, Xilinx, and Motorola microcontrollers
* Executive MBA – to enhance and expand our college wide center and our product engineering consortium (comprised of centers at four universities).
* HP82000 Mixed Mode IC Tester – One week course, at HP, CA, 1997
* On Improving Presentation Skills, at Harris, Melbourne, (1996), Two days.
* CDS/Cascade for retargetable cell library design, in Tempe, AZ, (1995), One week
* MEMS Fabrication, MCNC-sponsored conference, in Chicago, IL (1994).
* Design Automation Tools: Cascade Design Synthesis, Analogy for Mixed Mode Top-Down Design, and Comdisco/SPW for High Level Modeling, Motorola Sponsored (1993 & 1994), One week long courses each.
* Daizyx Design Automation courses, in San Jose, CA (1985), two week long.
* VLSI CMOS design course for professors at ISI, University of Southern California, CA (1985), two-week long.
	1. **Community Service**
* Developed smart phone Apps for health care, urban planning, science museum exhibits, and empowerment of middle school students, in collaboration with community stakeholders and university professors - high school and undergrad team projects, with interdisciplinary groups. Currently populating a **Github** open source site: <https://github.com/RShankar?tab=repositories> See also: <http://android.fau.edu/> , 2009-2014
* Judge, Science Fair, A.D. Henderson School, 2001-2003
* Judge, National Forensic League, Debating, High School Children, 2003.